CHARACTERIZATION OF A DIGITAL DATA ACQUISITION AND CONTROL SYSTEM FOR PHOTON-COUNTING IMAGING DETECTOR ARRAYS

by

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A Graduate Paper Submitted

in

Partial Fulfillment

of the

Requirements for the Degree of

MASTER OF SCIENCE

in

Electrical Engineering

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ROCHESTER, NEW YORK

MAY, 2012

Abstract

The design or modification of any system can introduce uncertainty in its operation, behavior, and limitations. This paper characterizes a modified data acquisition and control system originally designed by the MIT Lincoln Laboratory for a single imaging detector using a thermoelectric cooler. The new system, developed jointly between the RIT Center for Detectors and the MIT Lincoln Laboratory, expands this system to enable the simultaneous operation of four detectors within a vacuum-cryogenic dewar. The dewar is able to hold the detectors at a temperature of 70 K and the electronics at 175 K, which is far below the temperature rating of many semiconductor devices.

This paper discusses initial bench-top functionality testing of the newly designed Cold Fanout Board (CFB), full system Bit Error Rate (BER) testing as a function of clock frequency and temperature, and signal integrity analysis (simulations and hardware measurements). The testing showed that temperature had a minimal, if any, effect on operation. However, the system had significant errors at frequencies beyond 70 MHz, and it stopped functioning altogether at 80 MHz. Setting a fast FPGA slew rate increased the error threshold to 89 MHz, but ideally the system should operate up to 200 MHz.

Determining the source of the errors and attempting to find a solution consumed a significant portion of this project. Ultimately, the problem was reduced to an improperly routed clock net on the CFB. Various termination topologies were explored using Mentor Graphics HyperLynx simulations, but none were sufficiently practical to implement due to inner layer signal routing. Assuming funding availability and no time constraints, proper rerouting and simulation of the clock net is recommended.

Acknowledgements

I thank James Stefano of the Electrical Engineering Department, and Kenneth Garland and Chris Brown from the College of Applied Science and Technology for giving me permission to install and use the Mentor Graphics PADS PCB design suite, which includes the HyperLynx signal integrity simulation tool. Without their collaboration, I would not have been able to perform the simulations that defined much of this paper.

I also thank Jeffrey G. Lonneville at the Center for Electronics Manufacturing and Assembly for generously allowing my colleagues and I to use the surface mount soldering tools and X-ray equipment that allowed us to populate, modify, and inspect the electronic systems used throughout this project.

My advisor, Dr. Donald F. Figer, provided the laboratory space, equipment, and support that made this research possible. I have worked with Don and the Center for Detectors since March 2009. During that time, I have been privileged to work with a renowned detector scientist, and have gained experience far beyond what is taught in the classroom.

Tremendous thanks go to Brandon J. Hanold and Donald J. Stauffer for providing suggestions when I was stuck on a problem, sanity checks, and general detector and engineering guidance. Their expertise in detectors and electrical engineering have been invaluable.

And of course, I thank my parents, Douglas and Paula, for encouraging me to continue my education and always supporting me in my personal and academic endeavors.

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List of Acronyms

AC	Alternating Current.
APD	Avalanche Photodiode.
BER	Bit Error Rate.
CEMA	Center for Electronics Manufacturing and Assembly.
CFB	Cold Fanout Board.
CfD	Center for Detectors.
DB	Daughter Board.
DC	Direct Current.
DCM	Digital Clock Manager.
DLM	Dynamically-loadable Module.
FPGA	Field-Programmable Gate Array.
GM-APD	Geiger-mode Avalanche Photodiode.
IBIS	Input/output Buffer Information Specification.
IDL	Interactive Data Language.
JTAG	Joint Test Action Group.
LDO	Low Drop-Out.
LVDS	Low-Voltage Differential Signaling.
MIT	Massachusetts Institute of Technology.

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

NASA National Aeronautics and Space Administration.

PCB Printed Circuit Board.

PE polyethylene.

PSPICE Personal Simulation Program with Integrated Circuit Emphasis.

QRSS Quasi Random Signal Source.

RIT Rochester Institute of Technology.

RTT Round-Trip Time.

TDEM Technology Development for Exoplanet Missions.

TDR Time-Domain Reflectometry/Reflectometer.

TI Texas Instruments.

ULP User Language Program.

USB Universal Serial Bus.

UTP Unshielded Twisted Pair.

WEB Warm Electronics Board.

1 Introduction

This thesis characterizes a digital data acquisition and control system for the simultaneous operation of four Geiger-mode Avalanche Photodiode (GM-APD) array detectors. The detectors and electronic systems were designed through collaboration between the RIT Center for Detectors and the MIT Lincoln Laboratory as part of a research grant awarded by the Gordon and Betty Moore Foundation. While not explicitly part of the Moore project, thorough testing of the electronic system to understand its behavior and limitations is important to ensure the accuracy and reliability of the imaging data.

The findings from this characterization also have a direct impact on a second, but related research grant awarded by NASA for the Technology Development for Exoplanet Missions (TDEM)[1]. In the TDEM project, the detectors are irradiated with 60 MeV protons to a total dosage of 50 krad(Si), which is enough to simulate a typical 5-year dosage at L2 orbit[2]. Establishing a pre-radiation baseline of the imaging system is particularly important because the CFB will be exposed to secondary radiation, which may have adverse effects on the overall system performance.

1.1 System Overview

The acquisition and control system, shown in Figure 1, has several interconnected circuit boards that span between room-temperature (295 K) and a vacuum-cryogenic test chamber (dewar) operating with a detector temperature of 70 K and an electronics

[1]The Moore project funded development of a new zero read noise detector to enable the most sensitive observations with the World's largest telescopes, such as the Thirty Meter Telescope. The TDEM project is primarily concerned with the performance of these detectors in the presence of space radiation.

[2]The second Lagrange point (L2) orbit is approximately 1.5×10^6 km from Earth, and is beyond the orbit of the moon [1]. The L2 orbit is convenient because the gravitational pull from the Earth is small enough that spacecraft may remain at a constant distance for years with minor station-keeping maneuvers [1]

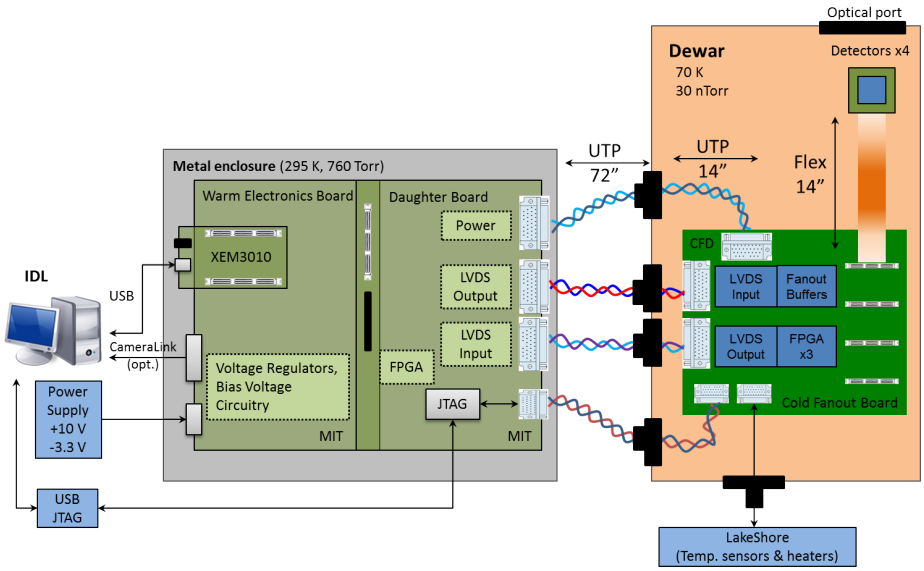
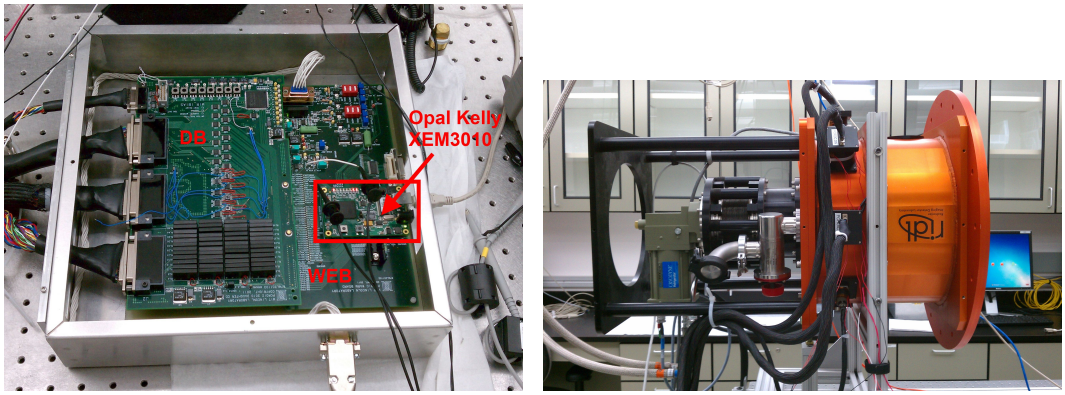


Figure 1: Diagram of the full system.

temperature of 175 K. On the room-temperature "warm" side, is the master FPGA located on an Opal Kelly XEM3010 development board. The XEM3010 is seated on the Warm Electronics Board (WEB), which was an existing design developed by the MIT Lincoln Laboratory for room-temperature testing of a single detector. In order to simultaneously test four detectors in a cryogenic environment, the Daughter Board (DB) was developed as an add-on to the WEB. The DB features an additional FPGA and the LVDS driver and receiver components for communication with the dewar electronics. The WEB and DB are directly connected as in Figure 2a using Samtec high-speed mezzanine connectors.

Within the dewar (Figure 2b) are the CFB and the detectors under test. Due to the initial design of the WEB and input/output pin limitations on the XEM3010, there are three, 100-position microminiature connectors on the DB and CFB. The interconnecting cables are Unshielded Twisted Pair (UTP) and are used for power, control signals to the detectors, and data output from the detectors. Each data cable provides 50 discrete signal paths to and from the cold electronics within the dewar.



(a) Warm Electronics Board (b) Dewar

Figure 2: (a) The interconnected WEB and DB; (b) the dewar, a cryogenic test chamber for the detectors.

The detectors are each 256x256 arrays of Avalanche Photodiodes (APDs) with more than 32 outputs per detector. Because of the high number of parallel outputs, the detector data must be multiplexed through the three FPGAs on the CFB before being output to the warm electronics.

The goal of the imaging system is to operate the four detectors simultaneously with a minimum detector master clock frequency of 20 MHz. There is no maximum specified clock frequency for the detectors, but ideally they would be operated as fast as the electronics allow in order to achieve high frame rates[3]. The design of the detectors is such that 16 bits of data are output for every two pulses of the master clock. Since the detectors are arrays of 256x256 pixels, and each pixel is represented by a single bit, a total of 8192 master clock pulses are required to capture a single frame. Therefore, a detector operating with a 20 MHz master clock will take 409.6 µs to output a single frame of data.

[3]The frame rate is the time it takes to read the contents of all the pixels (photodiodes) in an array. Because the detector is a GM-APD array (explained in subsequent sections), each pixel is represented by a single binary value: '1' indicates a photon was detected in a given pixel, and '0' indicates no photons were detected by that pixel.

Because the detector outputs are multiplexed through the CFB FPGAs, the FPGAs must be operated four times faster than the detector master clock in order for all the data to be received simultaneously by the acquisition computer. From this, it follows that the minimum clock frequency for the FPGAs is 80 MHz. The clock signals used in this system are generated by the Cypress CY22393FXC programmable clock generator on the XEM3010 development board. The CY22393FXC has a maximum rated output frequency of 200 MHz, which is also the maximum signaling frequency for the LVDS transceivers. Ordinarily an FPGA can implement a Digital Clock Manager (DCM) to synthesize arbitrary clock frequencies faster or slower than a given reference clock, but there is little reason to implement a clock synthesizer in this system because of the frequency limitation imposed by the LVDS transceivers. Assuming 200 MHz is attainable without errors, the corresponding maximum detector master clock frequency is 50 MHz, which produces a frame rate of 163.84 µs.

1.2 Photodetector Background

The PN Junction

The photodetectors in this project are based on the fundamental concept of a reverse-biased p-n junction, a diode. The p-n junction is created at the boundary between p-type and n-type doping profiles within the substrate of a semiconductor. The p-type region has an abundance of positive carriers, or holes—a lack of electrons; while the n-type region has an abundance of negative carriers, or electrons. These profiles can be established in several ways. In general, the substrate starts out lightly doped as p-type, and ion implantation accelerates the dopant atoms (usually n-type) into the substrate to reach the desired concentrations. Figure 3 shows a diagram of

the carrier concentration and electric field at each region in the substrate as a function of cross-sectional distance.

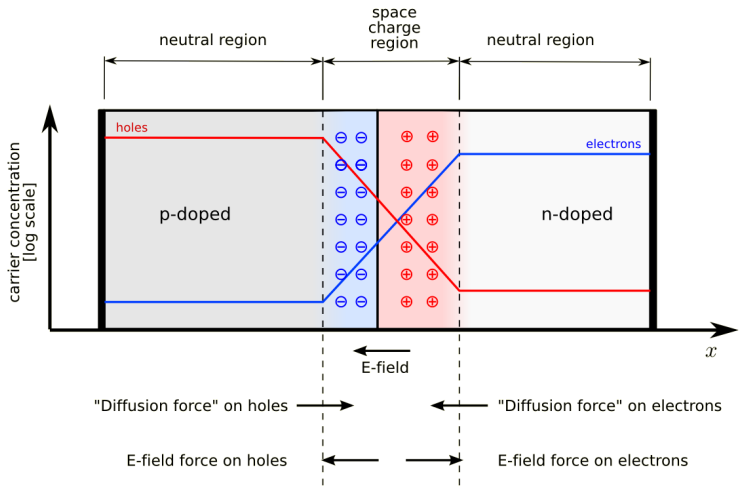


Figure 3: PN junction in thermal equilibrium and zero bias voltage [2].

The p-type and n-type regions at the extreme ends of the substrate are considered "neutral". At the p-n junction, electrostatic forces cause the electrons and holes to diffuse across the junction. This creates an electric field that resists further diffusion, and establishes equilibrium. The space charge (depletion) region is the area in which electrons and holes have diffused across the junction, and is so-named due to the absence of "free" carriers. Without the presence of an applied bias voltage across the junction, the natural diffusion of carriers creates a threshold, or built-in, voltage.

Many electronic applications take advantage of the p-n junction by applying a positive voltage to the p-type region, and a negative voltage to the n-type region. This places the diode into forward bias, compressing the depletion region to a point where electrons will start to flow into the p-type region, and holes into the n-type region. Once the bias voltage exceeds the built-in voltage, an electric current flows freely between the terminals of the p-n junction; below this threshold, almost zero current flows.

In reverse bias, however, a positive voltage is applied to the n-type region, and a negative voltage is applied to the p-type region. This increases the width of the depletion region, causing the device to become more resistive and the depletion region to behave similarly to a capacitor. If the magnitude of the reverse bias voltage becomes large enough, the device will break down causing a large, exponential "avalanche" current to flow across the device if free charge is available. If the magnitude increases unchecked, the device will overheat and become permanently damaged. This avalanche effect can have significant advantages in certain applications, however. Many devices are designed specifically to operate in and/or tolerate avalanche mode such as the Zener diode and the APD. The avalanche effect of an APD is especially useful for detecting faint objects in astronomy, where traditional photodiodes may be inadequate. APDs are also useful for laser ranging, adaptive optics, and are showing promise in telecommunications.

Detection of Light

Although there are many energy levels available to electrons within a crystal lattice, there are two energy bands of importance—the conduction band and the valence band. In a semiconductor, there exists a space between these energy bands called the band gap, where electrons are not allowed due to the crystal bonding structure of the material. An electrical conductor has virtually no band gap, and an insulator has a large band gap. The energy levels below the band gap are valence states, and the energy levels above the band gap are conduction states. Numerically, the band gap is the difference between the outer-most valence level, and the inner-most conduction level; it is the minimum amount of energy required to excite an electron from the valence band into the conduction band. Silicon, for example, has a

band gap of 1.1 eV, which allows for easy excitation of electrons into the conduction band.

There are two primary ways an electron can be excited into the conduction band: heat and light. In a photodetector, excitation by photons is the goal, while excitation due to heat is undesirable. Thus, photodetectors tend to be operated as cold as possible, usually with thermoelectric coolers or cryogenic refrigerators, which can maintain temperatures that approach absolute zero. This reduces atomic vibrations and minimizes the chance that electrons are excited into the conduction band.

$$\mathrm{E} = \frac{hc}{\lambda} \tag{1}$$

Equation 1 shows the relationship between photon energy (E) and photon wavelength (λ); h is Planck's constant, and c is the speed of light[4]. Excitation by light occurs when a photon enters the device substrate and ionizes an electron in the valence band, transferring its energy to the electron. If the energy increase is sufficient to overcome the band gap, the electron will jump into the conduction band, leaving behind a hole in the valence band. The electron, now in the conduction band, is able to move freely through the lattice structure of the material. Likewise, the hole travels through the lattice as surrounding electrons fill it.

In a reverse biased p-n junction, if the incident photon generates an electron-hole pair in the n-type region, the electric field of the junction pulls the hole toward the junction. If the electron-hole pair is generated in the p-type region, the electron is drawn toward the junction. In either case, both carriers move about somewhat randomly until either the energy dissipates and the electron falls back into the valence band (recombining with the hole undetected), or the appropriate carrier reaches the

[4]Planck's constant, $h \approx 4.136 \times 10^{-15}$ eV; and the speed of light, $c \approx 2.998 \times 10^{8}\,\mathrm{m\,s^{-1}}$.

p-n junction and is driven across into the oppositely-doped region where it recombines and reduces the stored charge of the junction.

$$Q = C \cdot V \tag{2}$$

An ideal p-n junction behaves similarly to a capacitor and thus stores a charge. Equation 2 is the steady-state equation for a capacitor; Q is the stored charge, C is the capacitance, and V is the voltage across the terminals. In order to detect a change in the stored charge of the junction, the p-n junction is initially charged to a known voltage approximately equal to the power supply and is disconnected using a MOSFET[5]. When a carrier makes it across the junction, it reduces the stored charge by 1 carrier ($\pm 1.602 \times 10^{-19}$ C). The difference between the initial charge and the final charge is amplified, thus providing an estimate of the amount of light that was collected. An important performance metric for photodetectors is the ratio of carriers that reach the p-n junction to the number of incident photons. This ratio is the quantum efficiency and is at best unity. However, losses due to reflection, absorption, and recombination outside the depletion region usually lower the quantum efficiency [3].

Ordinarily, the charge of a single electron is much too small to be accurately measured without being overwhelmed by various noise sources. In addition to thermal noise, read-out noise introduced by the amplifier MOSFETs that convert stored charge into voltage can have a considerable impact in photon-starved applications. There are a few solutions that attempt to amplify the signal before it reaches the read-out amplifiers. Photomultiplier tubes are one solution, but they are prohibitively

[5]For simplicity, it can be assumed that the initial voltage is equal to the supply voltage. In reality, due to atomic vibrations, timing jitter, and other imperfections, the initial voltage at the junction is slightly different each time the device is reset. Thus, the initial voltage is typically sampled immediately following a reset.

expensive and cannot be made small enough for use in photodiode arrays, especially large-format arrays that are becoming increasingly popular. Alternatively, increasing the exposure time is a simple way of accumulating more photons, but this reduces the overall system efficiency and can reduce image quality in dynamic scenes. Longer exposure times also cost more to operate—telescope time is limited, and time equals money. The APD overcomes these limitations because of its built-in gain.

The Avalanche Photodiode

An APD can be operated in two modes—linear and Geiger-mode. In linear mode, the p-n junction is reverse biased with a voltage magnitude below the breakdown voltage. This generates a strong electric field at the junction. When a photon of sufficient energy collides with the lattice structure and generates an electron-hole pair, the appropriate carrier is accelerated toward the junction with such force that it may collide with and displace additional carriers. The primary carrier, along with the secondary carrier(s), are again accelerated toward the junction, possibly creating additional electron-hole pairs in the process. This effect is known as impact ionization and is able to generate a significant avalanche current [3].

At some point, contention develops between the rate at which electron-hole pairs are created and the rate at which they are collected, or driven across the junction. If the magnitude of the reverse bias voltage is below the breakdown voltage (linear mode), collection wins and the avalanche terminates [3]. In this mode, the gain is proportional to the number of incident photons. However, the gain factor provided by the impact ionization effect is a statistical process, so while an average gain factor can be determined, the exact value changes—this is the multiplication noise [3]. The severity of the multiplication noise depends on the material properties of the photodetector since electrons and holes, in general, are not equally likely to initiate

impact ionization [3]. In silicon, electrons are much more likely to impact ionize than holes, thus keeping the multiplication noise lower than other materials, but still significant [3]. This problem is eliminated by operating the APD in Geiger-mode, which means the magnitude of the reverse bias voltage is beyond breakdown.

In Geiger-mode, impact ionization occurs much faster than collection. The greater the reverse bias voltage above breakdown, the faster the impact ionization multiplication occurs. Whether there are one or many incident photons, the result is the same, so an APD is usually operated in Geiger-mode in photon-starved applications. If the power supply could source infinite current, and there is zero series resistance between the terminals of the p-n junction, the multiplication would continue without bound [3]. In physical systems, however, there is always some small resistance. From Ohm's law, it follows that a constant resistance with increasing current flow results in a larger and larger voltage drop across the junction. This, in turn, reduces the voltage dropped across the high electric field region and slows the avalanche rate of growth [3].

A steady-state condition is reached in which the voltage across the high electric field region is reduced to the breakdown voltage, where the generation and collection rates balance out [3]. The series resistance provides a type of negative feedback that stabilizes the current level against fluctuations, making the concept of multiplication noise irrelevant [3]. Once in this state, the steady-state current would theoretically continue indefinitely until it is quenched. To put this another way, if a photon triggers an avalanche in a GM-APD, the photodiode saturates almost instantaneously. A device in saturation usually represents a '1' in a digital system, so the GM-APD has the additional advantage of being "purely digital", or "self-digitizing" and is thus less susceptible to external noise sources compared to analog detectors.

Quenching a GM-APD can be accomplished using passive or active circuitry. Passive quenching is somewhat similar to the basic photodiode in that the APD is initially charged to some voltage above breakdown and left in an open-circuit configuration. When a photon of sufficient energy generates an electron-hole pair that initiates an avalanche, the flow of current within the photodiode discharges its internal capacitance until the stored voltage is no longer above breakdown, thus causing the avalanche to terminate [3]. On the other hand, an active quenching circuit senses when the APD starts to self-discharge, then quickly discharges it to below breakdown with a shunting switch [3]. Passive quenching is very simple, but it is much slower than the more complicated active quenching circuits. The type of quenching circuitry is usually determined by the target application.

An important point to note about semiconductor devices that has a direct impact on photodiodes, and APDs in particular, is the problem of trapping. Traps are discrete carrier energy states created by defects within the lattice structure of the device substrate. Defects can be in the form of contaminant atoms (impurities), or lattice defects such as voids or interstitial atoms. In an APD, these traps can be a source of false photon counts. For example, when an avalanche is quenched, not all of the carriers are collected—some remain behind, possibly within a trap. Because of thermal energy, carriers are always vibrating. At some point, the trapped carrier may be dislodged, accelerate toward the high field region, and trigger a secondary avalanche in the process. This is called afterpulsing and is indistinguishable from a photon event, thus it can be a major problem for highly sensitive imaging applications. Often, afterpulsing is controlled with improved device fabrication techniques, sufficient cooling, better quenching circuits, and adequate hold-off times before re-arming the APD.

2 Initial Setup and Testing

Initial testing for this paper was focused on the Cold Fanout Board because the Daughter Board was previously tested for proper functionality. This testing was important to ensure that there were no manufacturing defects and that the CFB operated as intended. If this phase of testing was not completed, and the CFB was initially connected to the system, there easily could have been catastrophic damage if certain design flaws or manufacturing defects were present. This is applicable to nearly every design.

Therefore, after the blank CFB PCBs were received from Sierra Circuits, a quick visual inspection was performed to ensure that there were no major manufacturing defects such as bubbling/separating FR4 layers, bad copper pours, or inaccurate drill hits. Next, a basic continuity check was performed to verify that there were no short circuits between critical nets such as the power rails and ground. After reasonably ensuring that the blank PCBs were properly fabricated, the next steps were manual component placement and bench-top functionality testing.

2.1 Component Placement

Many of the components on the CFB are fine-pitch (0.5 mm and smaller), which made the placement difficult, but possible. The surface-mount tools available in the CEMA laboratory at RIT were invaluable during this process. For most components, all that was required was a fine tip on the solder paste dispenser and a moderately steady hand. Some of the more difficult components to affix to the CFB were the high-speed mezzanine (Samtec QTH) connectors for each of the detectors, the Spartan-3AN FPGAs, and the SN74LVC16244A-DGG buffer chips.

After one or two failed attempts, an interesting process was established for attaching the Samtec connectors (refer to Figure 4). First, solder paste was applied to the pads for the central blade pins. The Samtec connectors were then carefully placed on the board and the solder was cured using a Metcal reflow station[6]. The blade connections were verified using the Glenbrook Technologies Jewel Box 70-T X-ray machine, and electrical continuity checks ensured no short circuits were formed.

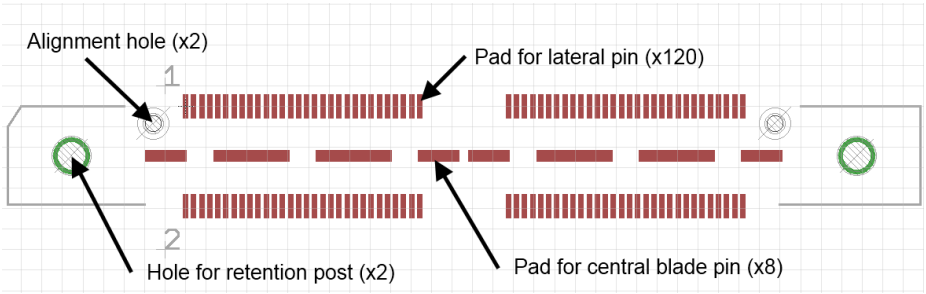


Figure 4: PCB footprint for the Samtec QTH high-speed mezzanine connectors. These connectors feature pins with 0.5 mm pitch, and retention posts for secure mating with the Samtec QSH connectors on the detectors.

Once it was certain that the central blades were attached and properly connected, the retention posts were soldered using standard solder and an iron. The final step was simple because the lateral pins of the Samtec connectors sat slightly above the pads, providing a small air gap. The fine tip on the solder paste was able to inject solder between the pad and the pin, and due to surface tension, the paste had a tendency to not bleed over to the neighboring pins[7]. Any bleeding that did occur was minimal and when the solder was cured at the Metcal reflow station, the surface tension of the molten solder automatically cleared any bridges.

[6]Because only the central blade connections had solder paste, a perfectly steady hand was not critical.

[7]If the solder paste was applied first, there was far too much bleeding between pins, which quickly became messy. Additionally, it would require an extremely steady hand or a special tip for the Metcal pick-and-place tool (not available) in order to place the connector without smudging the paste onto neighboring pins.

The FPGA chips were populated with careful application of solder paste to each pad; but being standard quad flat packages, the chips themselves were placed using the Metcal pick-and-place tool. This saved time and was more reliable than hand placement. The connections were verified using the Glenbrook X-ray machine, and electrical continuity checking ensured no short circuits between the power rails and ground.

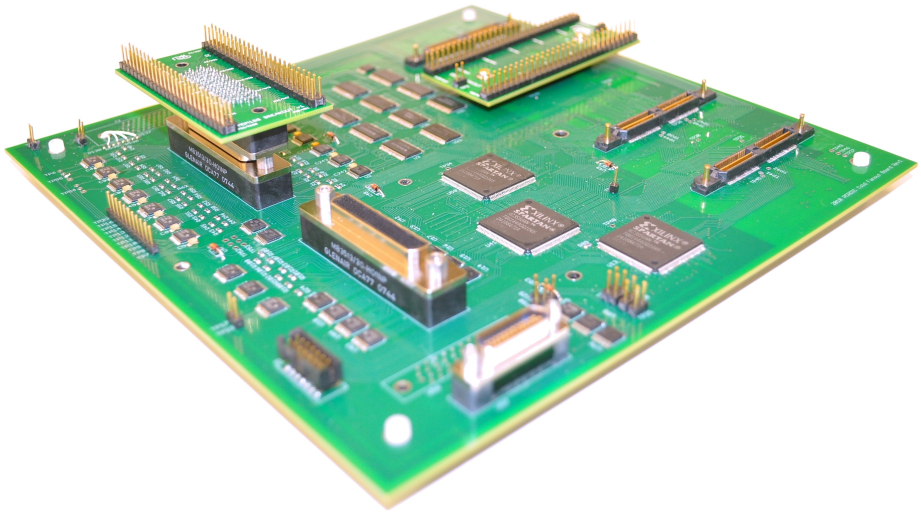


Figure 5: Cold Fanout Board.

The LVC16244 buffers were applied in a similar manner, but had to be placed manually. This created several solder bridges that were removed using a narrow splinter formed by breaking the wooden handle of a cotton swab. After all components were placed, the board was given a final inspection under the Glenbrook X-ray machine, and quick electrical testing ensured that there were no short circuits between the power rails and ground. The nearly completed CFB is shown in Figure 5.

2.2 Bench Testing

Initial bench testing is critical to ensure basic functionality of the CFB. In this phase, the board was powered on and the current draw display was monitored for excessive current draw. Using the device datasheets as a guide, the total device current draw for each rail should be no higher than 500 mA under full load. After the board was successfully powered up, JTAG communication with each FPGA was verified with the Xilinx ISE iMPACT software, and a rudimentary clock divider circuit was programmed onto each FPGA. Finally, the LVDS transceivers and buffers were tested individually to ensure that all components were properly functioning.

For the power-up and current draw tests, an Agilent E3648A power supply was configured to output 3.3 V and 1.2 V on each output. The current limit on both outputs was set to 500 mA. The CFB was powered through test points TP1 (3.3 V) and TP2 (1.2 V). The 3.3 V supply registered 253 mA, and the 1.2 V supply registered 6 mA. These were reasonable current measurements because the 3.3 V supply powers all the transceivers and buffers, and even though they were idle, they still consumed power. The 6 mA on the 1.2 V supply is also reasonable because it powers the V_{CCINT} pins on the FPGAs, which were not programmed and thus drawing minimal power.

Next, the JTAG chain was tested by connecting the Xilinx JTAG cable to the X1 header. Initialization of the chain by ISE iMPACT was successful as each of the three FPGAs were recognized. From the layout of the CFB, the JTAG chain device order is: U41, U58, and U13. Each device was assigned a configuration file, but only the last device (U13) was programmable. ISE iMPACT reported that it could not pull the DONE pin high. (Refer to Appendix A for a description of the Spartan-3 JTAG configuration pins). The "Generate Programming File" settings in the ISE projects

for each FPGA were edited such that the PROG and DONE pins were set to float after programming. However, this did not rectify the problem.

On page 55 of [4] is Figure 6. This is the recommended DONE and INIT_B configuration for daisy-chained or broadside JTAG connections. The CFB was designed following this recommendation, except it used 1.0 kΩ pull-up resistors on the ganged DONE and INIT_B outputs instead of 330 Ω and 4.7 kΩ as shown. It could be that this difference was enough to interrupt proper JTAG programming, but this was never investigated. As mentioned in the user guide, the purpose of the 0 Ω resistors at the DONE and INIT_B outputs is to provide a means to isolate individual FPGAs for debugging purposes [4]. This means that disconnecting an FPGA from the common DONE signal allows it to be programmed individually via the serial or JTAG interface [4]. Thus, all six 0 Ω resistors were removed from the DONE and INIT_B pins on the CFB, and programming was successful for all FPGAs.

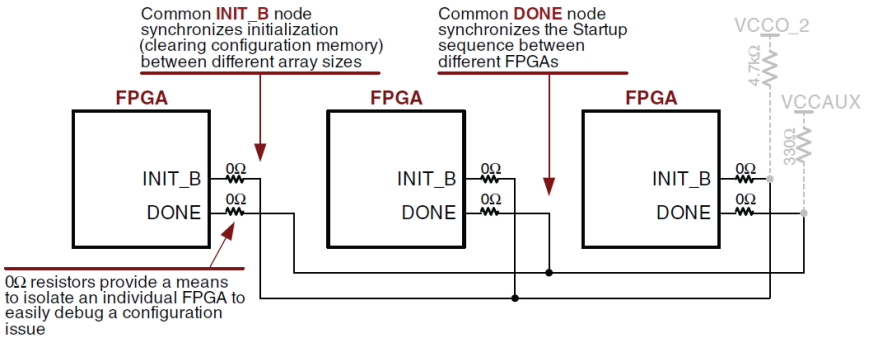


Figure 6: Xilinx User Guide 332 recommended DONE and INIT_B pin configuration for daisy-chained or broadside JTAG configurations [4]. The CFB was designed in a similar manner, but used 1.0 kΩ pull-up resistors on the ganged DONE and INIT_B outputs instead of 330 Ω and 4.7 kΩ as shown in the figure.

The initial FPGA programming was a simple clock divider. The FPGAs were given a 10 MHz clock signal and were programmed to output a copy of the input clock, a half-rate version, and a quarter-rate version. The Opal Kelly XEM3010 was modified to output LVDS signals and was connected to the BRK3010 breakout board.

The XEM3010 was programmed to generate the 10 MHz clock used by the CFB FPGAs. Once correct operation of the FPGAs was verified, they were reprogrammed with the system code that multiplexes the signals from each detector output to a single 100-pin microminiature connector, FPGA_DOUT. The breakout boards shown in Figure 7 were used at the FPGA_DIN, FPGA_DOUT, and Samtec connectors to provide convenient full board verification.

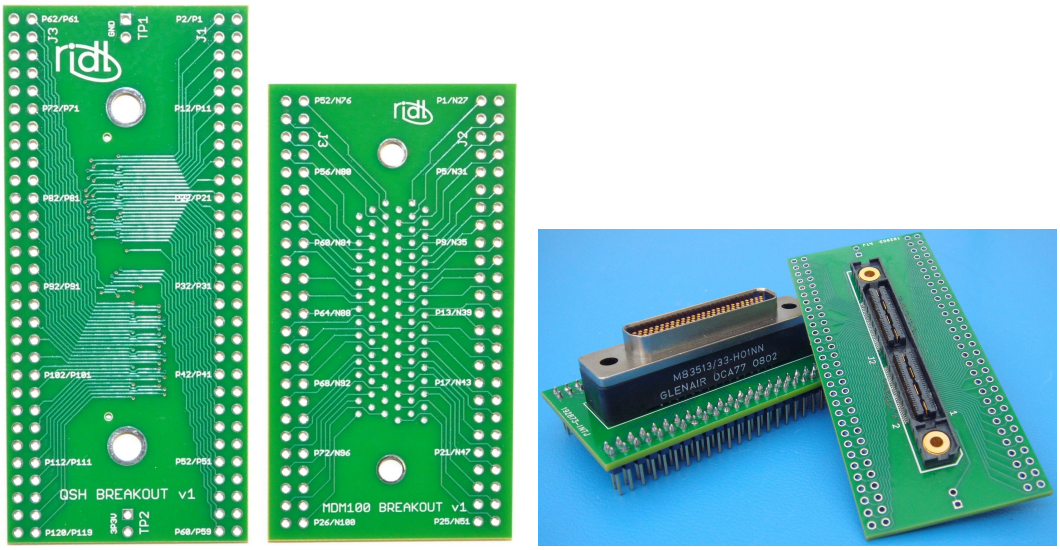


Figure 7: Custom breakout boards designed for the Samtec QSH and M83513 100-position microminiature connectors.

Full board verification followed the loop-back structure shown in Figure 8. The Opal Kelly XEM3010 was programmed to output an LVDS clock signal, which was applied to each of the inputs at the FPGA_DIN connector on the CFB. These signals were converted to single-ended via the Texas Instruments SN65LVDS048APW LVDS receivers, passed through the Texas Instruments LVC16244 buffers, and ended at each of the four CFB Samtec connectors. A short jumper wire was used to connect these detector control inputs to the detector data output pins, which connect directly to the three FPGAs. The FPGAs multiplex the four versions of the detector data signals, and output them one-at-a-time to the Texas Instruments SN65LVDS047A

LVDS drivers; these LVDS signals are monitored at the FPGA_DOUT connector on the CFB. In this manner all inputs and outputs were successfully verified for proper functionality.

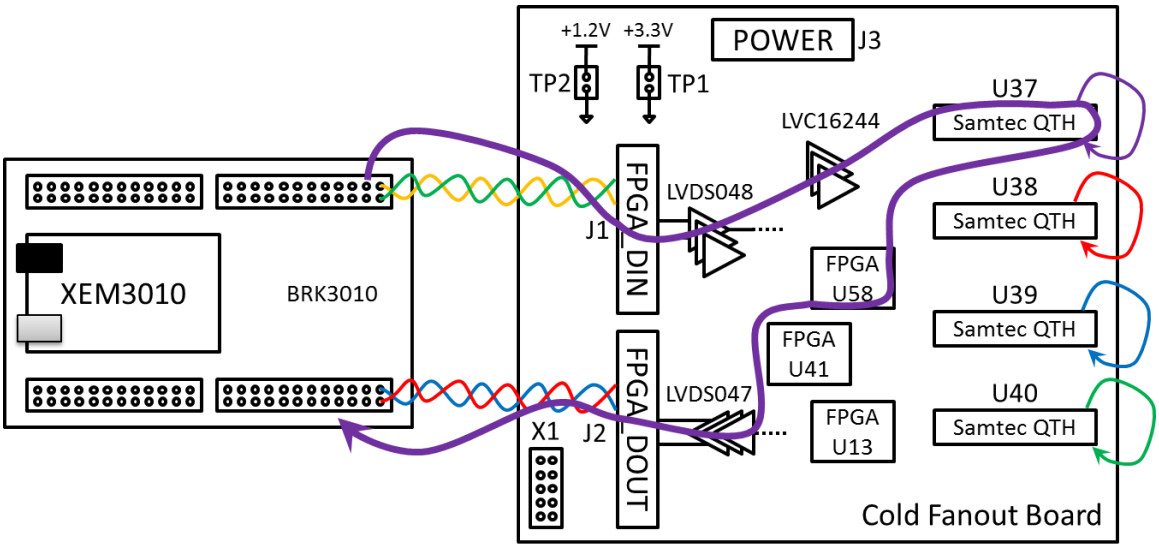


Figure 8: Cold Fanout Board loop-back test setup. The thick purple arrow is an example signal path. Note that the loop-back test verifies the functionality of each component on the CFB. This general setup was also used during BER testing.

3 Bit Error Rate Testing

Bit error rate (BER) testing is common in many of today's high-speed digital communication systems [5–7]. It is important because it quantifies the performance of the transmitter, receiver, and communication medium in terms of a single, unitless ratio: the number of erroneous bits to the total number of bits transmitted. The setup for a BER test is straightforward: a controller sends a known bit stream across the communication medium into the device under test, and ideally the device under test returns the exact same bit stream to the controller. The controller compares the original bit stream to the returned bit stream and any differences are recorded as bit errors.

Some applications, such as voice communication, can tolerate bit error rates up to 10^{-3}, while data transfers should have error rates less than 10^{-9} [8]. As a result, many data transfer protocols utilize parity functions that correct minor errors. However, the imaging electronics being characterized in this project do not have any form of error checking or parity. This means that the system must not only support high data rates, but also have zero errors at these speeds[8]. To determine the accuracy of the imaging system communication channels, several BER tests were devised.

3.1 Selected BER Test Patterns

There are many bit stream patterns used in BER testing, most of which were created to imitate various worst-case scenarios for a given protocol. This section outlines some of the patterns used in this experiment.

[8]The theoretical maximum output is 32 bits in parallel operating at 200 MHz; however only 16 of these bits are planned on being used at any given time.

Pseudorandom Binary Sequence

The pseudorandom binary sequence is simple to implement and the most generic pattern. Because of the random nature of errors, the pseudorandom sequence helps to shorten the time required for obtaining reliable BER measurements [5]. Another useful feature for the pseudorandom sequence is that it can be used for creating eye diagrams, which is discussed later.

Although not used in this experiment, a similar pattern is Quasi Random Signal Source (QRSS), which is a pseudorandom sequence with certain restrictions. Generally, QRSS is a 20-bit sequence that repeats every $2^{20} - 1$ bits and consecutive zeroes are limited to no more than fourteen [6, 7]. QRSS is more commonly used for testing T1 lines because the unconstrained pseudorandom pattern violates the ones density and/or consecutive zeroes restrictions for T1 signals [6].

Simple Counter

The simple counter is a counter that starts at zero and increments by one at each clock cycle. This is not necessarily a common industry pattern, but it was simple enough to implement and was used to quickly establish whether the BER algorithms and FPGAs were functioning properly.

Alternating ones/zeroes

The alternating ones/zeroes pattern is also non-standard, but it was used as a simple method for testing crosstalk interference between adjacent signal paths. It also provided a means to test for excessive signal path skew. Because each signal path was programmed to alternate between one and zero, any delays relative to the rising edge of the clock would be easily detectable.

Other patterns

When researching BER patterns and BER test methodologies, most of the results were designed for testing T1/DS1 communication channels. Although possibly useful for other applications, many of the BER patterns were designed to trigger certain failure modes. Some of the potentially useful patterns include "3 in 24", "1 in 8" or "2 in 8", and "all-ones".

The "3 in 24" pattern is a 24-bit pattern that contains at most three ones, and the longest string of consecutive zeroes is fifteen [6]. The "1 in 8" and "2 in 8" patterns are similar in that there is only one or two ones in a string of eight bits. These patterns are primarily used for testing clock recovery in T1 systems [6].

The all-ones pattern is a static string consisting of all ones. It is useful for stress-testing the communication components because the maximum power is consumed [6, 7]. Similar to the all-ones pattern, the all-zeroes pattern is a static string of zeroes. However, its usefulness is unclear beyond violating the maximum consecutive zeroes restriction in a T1 system.

3.2 BER Test Results

The BER tests in the following sections were performed using the Verilog hardware description language targeted for Spartan-3 FPGAs. The data read-out and FPGA control was achieved using the Interactive Data Language (IDL). IDL is a proprietary programming language currently owned by Exelis (formerly ITT); it is primarily used for scientific visual data processing in astronomy. Unlike most programming languages, IDL is optimized for array-based operations and is most similar in function to MATLAB. USB communication with the XEM3010 FPGA is achieved using a C library provided by Opal Kelly. IDL provides several methods of extending its

functionality by interfacing with external programs, the preferred method at CfD is the use of Dynamically-loadable Modules (DLMs) [9]. A DLM provides the necessary interface for IDL to call FORTRAN and C code [9]. Implementing a DLM can be difficult, but it was successfully accomplished for the Opal Kelly USB library.

The general BER test setup used in the following scenarios swept the data clock frequency through a selected range with a step of 1 MHz. The U13, U41, and U58 FPGAs respectively had 7, 16, and 8 signal paths that were tested simultaneously[9]. On each clock cycle, the logic level on each path changed according to the selected BER pattern. A single BER iteration sent and received 1 kbit of data per signal path. The CFB FPGAs were tested simultaneously with the same test pattern.

Bench Setup

The first BER tests were performed on the bench using the XEM3010 FPGA as the controller. The setup was similar to that shown in Figure 8. The XEM3010 was interfaced with the BRK3010 breakout board to simplify wiring to the CFB. The XEM3010 was configured to use the basic counter BER pattern, which was output over LVDS twisted pair wiring to the FPGA_DIN connector of the CFB. The FPGAs on the CFB sent this data back to the XEM3010 through the FPGA_DOUT connector and LVDS twisted pair wiring. The frequency range was 5 MHz to 30 MHz with 1 MHz steps. At each frequency, 30 BER test iterations were performed.

The results of this test are shown in Figure 9. The error rate should be zero at these frequencies, but it is evident that the error rate is between 50% and 100%, which is unacceptable. The high error rate was attributed to mismatched termination on the XEM3010, which was configured for 50 Ω signals. The LVDS drivers on the CFB are optimized for 100 Ω termination. Instead of changing the resistors on the

[9]This is due to the design of the CFB and the signals multiplexed by each FPGA.

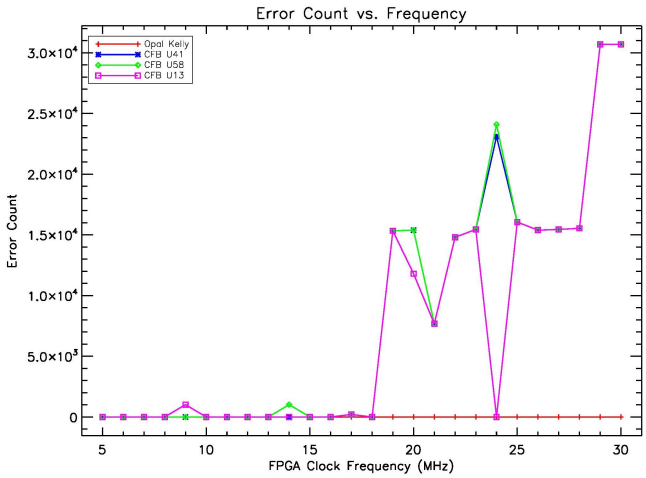


Figure 9: Initial bench-top CFB BER test results. The XEM3010 FPGA was directly controlling the CFB. This setup used the binary counter BER pattern from 5 MHz to 30 MHz with 1 MHz steps and 30 test iterations at each step.

XEM3010 and/or reconfiguring digitally controlled impedance, it was easier and more practical to test the CFB as it was designed—with the WEB and DB.

Dewar Setup

Because the bench setup was not how the system was designed to be operated, it is possible the errors were caused by the setup itself. To test this, the BER tests were repeated using the full system setup, complete with the WEB, DB, and dewar connections. The setup diagram was similar to Figure 8, but instead of the BRK3010, the XEM3010 was interfaced with the WEB/DB. The results using the counter pattern are shown in Figure 10. To speed up data processing, only the U58 FPGA was tested. The frequency range for this test was 1 MHz to 73 MHz with 1 MHz step. At each frequency, 5 BER test iterations were performed.

Figure 10 shows that errors continued to exist, but upon further inspection of the data, the failure mode was different from the bench setup. In this case, all data were

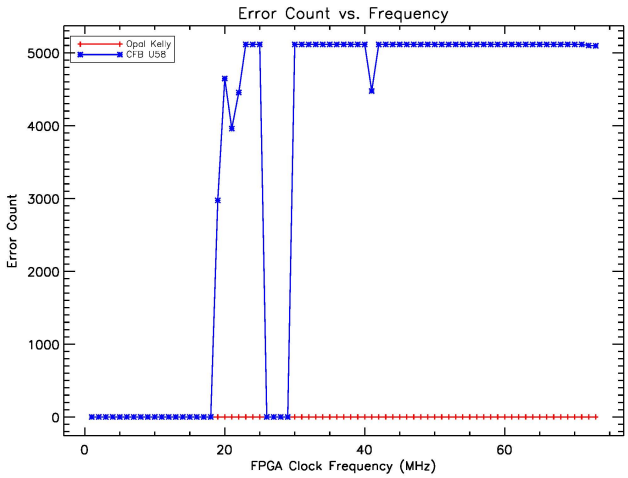
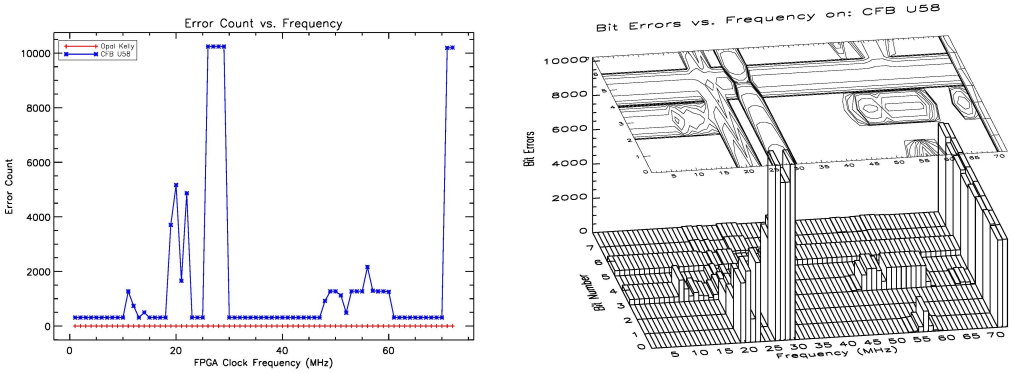


Figure 10: BER test results with the full system setup using the binary counter pattern from 1 MHz to 73 MHz with 1 MHz steps and 5 iterations at each step.

delayed by one clock cycle starting at 19 MHz. The delay increased to three clock cycles by 70 MHz, and there appeared to be missing data above 70 MHz.

Although perhaps not the ideal solution, the data delay was corrected by sending an additional signal to the CFB FPGAs; this signal was returned to the XEM3010 along with the BER data. The theory was that this signal would have a similar delay compared to the BER data, so when this signal was received by the XEM3010, the XEM3010 would know when to start recording. The BER test was repeated using the same parameters as before, but with 10 iterations per frequency step. Figure 11 shows that the addition of the delay signal significantly improved BER results. Instead of a nearly constant 100% error rate at frequencies above 20 MHz, the delay signal reduced the error rate to a maximum of nearly 25% between 30 MHz and 70 MHz.

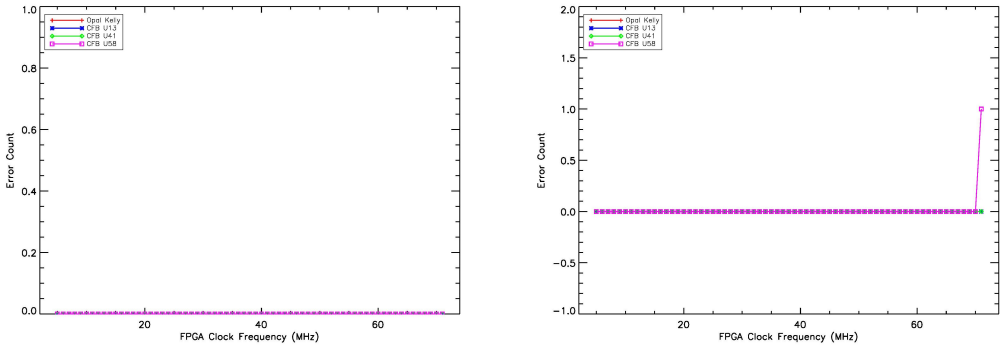
The 3-D plot shown in Figure 11b suggests that the BER failures had a tendency to occur more on certain signal paths (e.g. bits 3 and 5) than others. From this, it was hypothesized that there was excessive skew on these paths. Skew measurements were obtained with an oscilloscope and it was found that the worst-case skew was



(a) Overall (b) Bit-level contour plot

Figure 11: Full-system BER results with delay signal. (a) Shows the overall error count per device under test; (b) shows the 3-D contour plot for CFB FPGA U58 and shows which bits are erroneous.

nearly 1 ns between the fastest and slowest path. It was also found that bits 3 and 5 were the slowest paths.



(a) Counter pattern (b) Pseudorandom pattern

Figure 12: Full-system BER results with delay signal and DCM.

Implementing a DCM on all FPGAs introduced enough of a delay on the clock signal that all skew-related errors were eliminated. BER tests were repeated over a frequency range of 5 MHz to 71 MHz with a step of 1 MHz and 20 iterations per step. This time, two test patterns were used: a binary counter (Figure 12a) and a

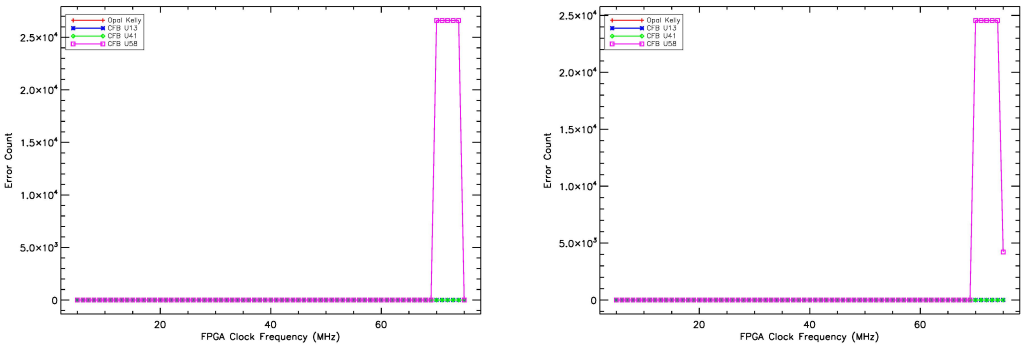
pseudorandom binary sequence (Figure 12b). Zero errors were recorded when using the binary counter pattern, but the pseudorandom pattern revealed a single bit error on CFB FPGA U58 at 70 MHz.

Temperature Ramp-down

Once it was established that the BER tests were operating reasonably well, the temperature of the dewar was ramped down from 295 K to 186 K. The temperature controller was configured to hold the detectors at 295 K. This introduced enough thermal load that it prevented the CFB from reaching lower temperatures.

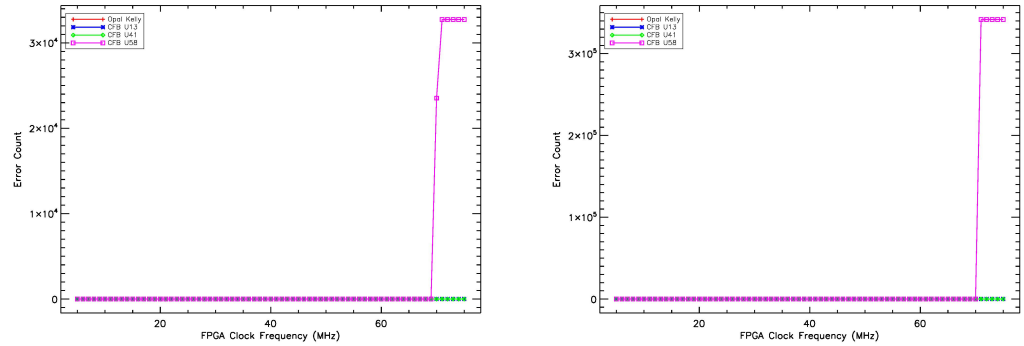
The BER testing in this scenario was performed over a frequency range of 5 MHz to 75 MHz with 1 MHz steps. During this test, the frequency was incremented after a single BER iteration, and the number of iterations was left unbounded. Once the maximum frequency limit was reached, the frequency would be reset to the minimum value and the test would continue with the next iteration. In this manner, a total of 418 iterations were recorded over 24 hours. Figure 13 shows the entire temperature range divided into four segments: 294 K–268 K, 267 K–241 K, 240 K–214 K, and 213 K–186 K. Because the CFB temperature decreased asymptotically, the lower temperature ranges generally have more BER iterations[10]. For example, the 294 K–268 K range completed 24 iterations, and the 213 K–186 K range completed 335 iterations. Compared to the baseline BER results at room temperature (Figure 12), no abnormal errors were observed.

[10]This is acceptable in this case because no abnormal errors were observed (compared to the baseline BER tests at room temperature). Otherwise, the BER plotting code was written such that the range window can be changed if necessary.



(a) 294 K > T ≥ 268 K

(b) 268 K > T ≥ 241 K



(c) 241 K > T ≥ 214 K

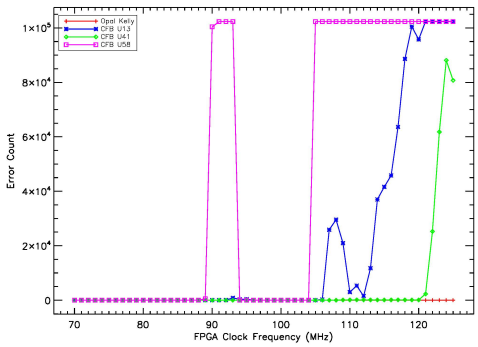
(d) 214 K > T ≥ 186 K

Figure 13: Full-system BER results versus temperature. The first temperature range (a) completed 27 BER iterations. The second temperature range (b) completed 24 iterations. The third temperature range (c) completed 32 iterations. The final temperature range (d) completed the remaining 335 iterations.

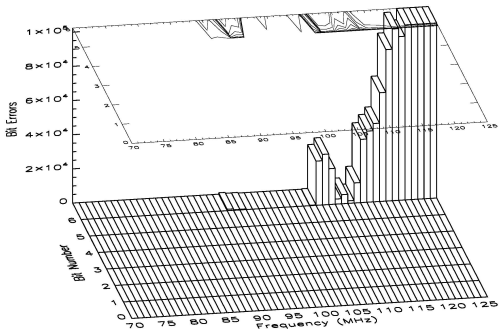
FPGA Slew Rate: Fast

By default, Xilinx ISE sets the output pin slew rate to "slow" in order to reduce noise, but this has the side effect of limiting the maximum output frequency. The slew rate can be configured in a single line within the Xilinx ISE project user constraints file and has two options: "slow" and "fast". The slew rate was changed to "fast", and the BER test was repeated. This time, the frequency ranged from 70 MHz to 125 MHz with 1 MHz steps. At each step, 100 BER iterations were performed using

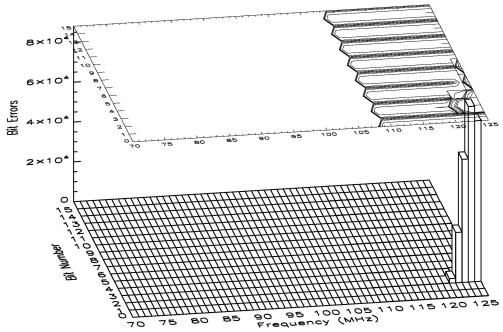
the alternating ones/zeroes pattern. As the results in Figure 14 show, the "fast" slew rate had a strong positive effect. Instead of the system failing with 100% error rate on U58 at nearly 70 MHz, system failures began appearing at 89 MHz.



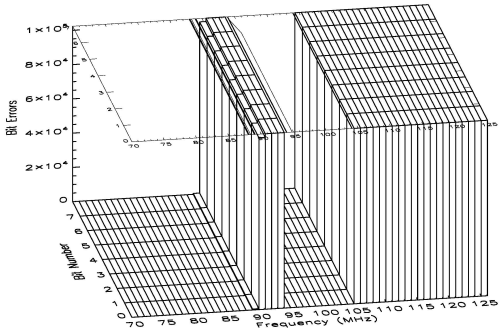
(a) Overall Results



(b) CFB U13



(c) CFB U41



(d) CFB U58

Figure 14: Full-system BER results with fast slew rate. The data were gathered using the alternating ones/zeroes pattern across a frequency range of 70 MHz to 125 MHz with 1 MHz steps and 100 iterations per frequency step. The plot in (a) shows the overall system results, while the plots in (b), (c), and (d) show the bit-level results for each FPGA on the CFB.

4 Signal Integrity Analysis

This section explores a variety of signal integrity analysis techniques to determine the cause of the bit errors previously observed. These techniques include eye diagrams, a thorough investigation of the twisted pair cabling and its effects on signal quality, and OrCAD PSPICE and Mentor Graphics HyperLynx simulations of the cabling as well as select PCB traces on the CFB. A combination test board was also designed for obtaining time-domain reflectometry measurements, and for testing the performance of the LVDS transceivers separate from the system.

Throughout this section, several references are made to various signal names in the system. Figure 15 is a detailed system diagram that attempts to clarify the signal names and their general paths through the system.

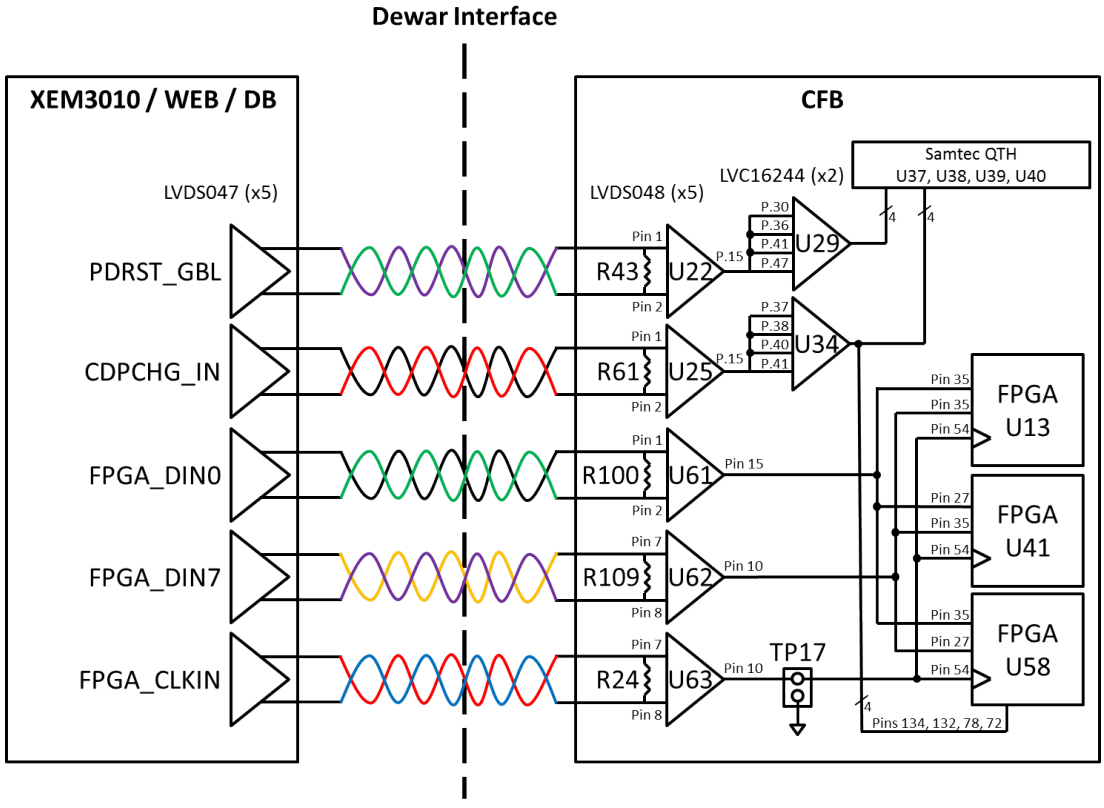
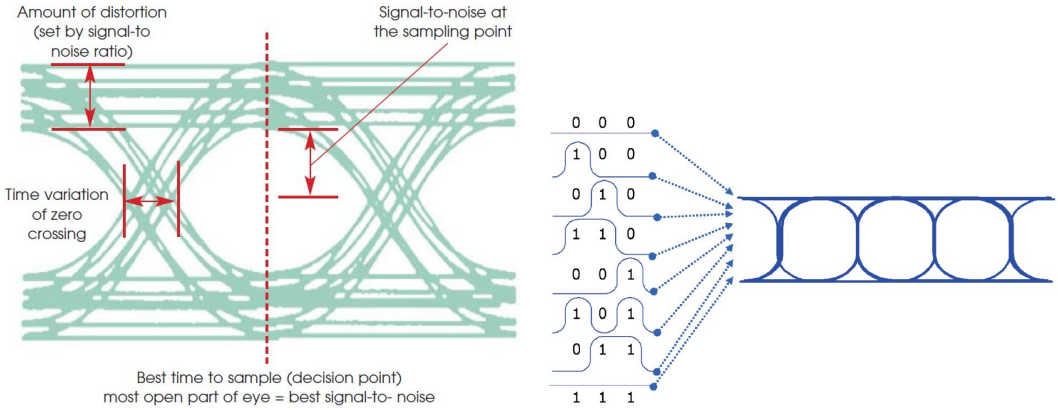


Figure 15: Imaging system signal path diagram for signal integrity analysis.

4.1 Eye Diagrams

Eye diagrams are useful in signal integrity analysis because they provide a qualitative means of determining the quality of a communication channel and can offer insight into imperfections along the signal path [10, 11]. A basic eye diagram is constructed with the design under test and an oscilloscope. The design under test is programmed to output a clock signal and a pseudorandom binary sequence. The oscilloscope is triggered with the clock signal, and the pseudorandom sequence is monitored [11]. The result is a pattern that looks like a series of eyes, as in Figure 16. A properly constructed eye diagram should contain all possible bit sequences, including long strings of consecutive ones or zeroes [11].



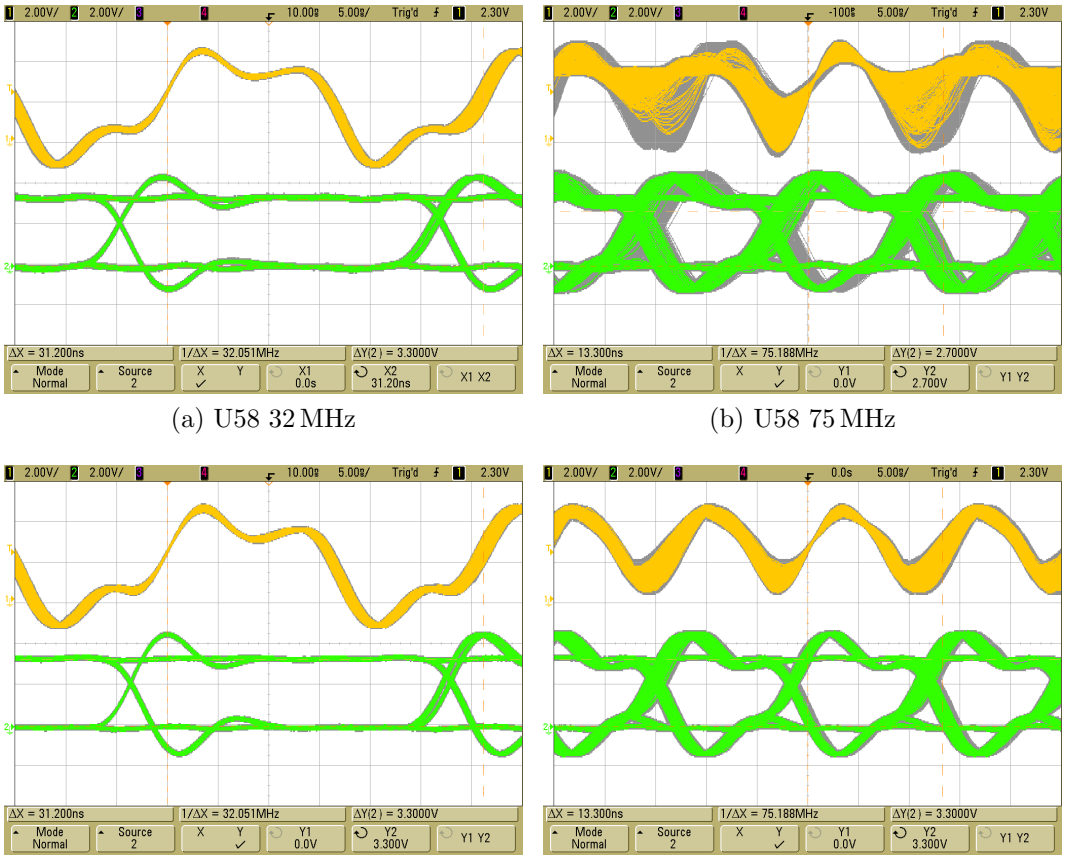
(a) Qualitative information contained in an eye diagram

(b) Overlay of bit sequences that form an eye diagram

Figure 16: (a) Shows the qualitative information contained in an eye diagram. The most important are the vertical eye opening (noise) and the width of the crossing point (jitter) [10]. (b) Shows an overlay of the bit sequences that form an eye diagram [11].

The full system was configured for an eye diagram test by programming the XEM3010 FPGA to output a clock signal over FPGA_CLKIN, and a 32-bit pseudorandom sequence over FPGA_DIN7. The Agilent MSO6032A oscilloscope was setup to trigger on the clock signal (channel 1) while monitoring the data signal (channel 2). A sampling of eye diagrams is shown in Figure 17. During this test, the FPGAs were

configured with the default (slow) slew rate[11]. With that setting, the U58 FPGA was considered to be the worst case (highest error rate), and the U13 FPGA was considered to be the best case (lowest error rate).



(a) U58 32 MHz (b) U58 75 MHz

(c) U13 32 MHz (d) U13 75 MHz

Figure 17: A sampling of eye diagrams using the full system. Channel 1 (yellow) is the FPGA_CLKIN clock signal, and channel 2 (green) is the eye diagram formed by the pseudorandom sequence. The U58 FPGA was considered worst case and the U13 FPGA was considered best case. Both reside on the Cold Fanout Board.

Because the BER testing showed failures at frequencies above 70 MHz, it was expected that the eye diagrams at these frequencies would exhibit significant jitter (tens of nanoseconds) and a small vertical eye opening (less than 2 V peak-to-peak),

[11]The eye diagrams were captured early in the testing phase, before the FPGA slew rate was changed to "fast". When using a fast slew rate, FPGA U41 is actually the "best case" because it had the lowest error rate.

if any opening at all. The eye diagrams captured in Figures 17b and 17d were not as bad as expected. At 75 MHz, the worst-case (U58) jitter was approximately 4 ns, and the vertical eye opening was approximately 2.7 V. At the same frequency, the best case (U13) showed a much better eye with an opening of 3.3 V and a jitter of about 1.5 ns. However, in both 75 MHz cases, the clock signal (channel 1) was highly degraded. In this system, an ideal clock would be a square waveform with equal time in the logic low and logic high states and have less than 1 ns jitter. In Figure 17b in particular, the clock signal was not consistently able to reach the logic low threshold voltage of 800 mV, which would cause increased error rates.

4.2 System Cable Simulations

The BER test results reveal that there were significant communication problems at frequencies beyond 70 MHz. The errors appeared more often on some signal paths than others, so one of the first suspects was the UTP cabling because it was twisted using a cordless drill and hand-soldered. The concern was that the soldering was performed by people of various skill levels, and the amateur twist job produced twist rates that varied significantly—from very loose to somewhat tight. In practice, it is generally a good idea to slightly vary the twist rate within bundled UTP cabling because it reduces the possibility that neighboring pairs will consistently have the same wires facing each other as demonstrated in Figure 18. If this occurs, it may introduce more crosstalk interference on one wire than the other wire within a pair. Such interference may not be sufficiently canceled out by the receiver.

However, if there is too much variation in the twist rates, the characteristic impedance of the wire pairs can be dramatically different. A pair that is loosely twisted provides more freedom for the individual wires to separate, which changes

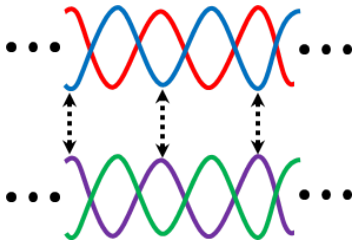
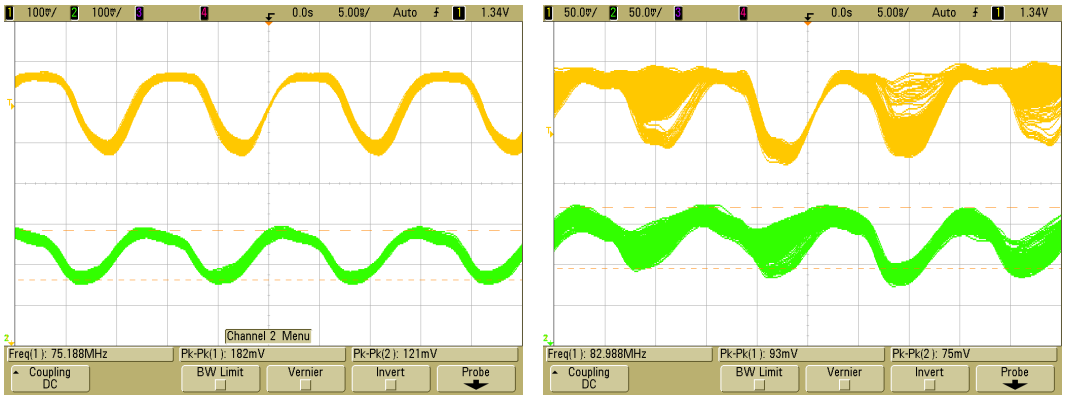


Figure 18: Two neighboring twisted pairs of the same twist rate.

the effective permittivity[12] and can have a significant effect on the characteristic impedance [12]. Because the termination used in this system is a fixed 100 Ω resistor for all pairs, any pair with a characteristic impedance that deviates from 100 Ω will experience greater interference due to signal reflections. Thus, the cabling became the first target for investigation and initial oscilloscope testing seemed to support this theory.



(a) 75 MHz (b) 80 MHz

Figure 19: Oscilloscope captures across the system cabling. The yellow trace (channel 1) is probing the positive output of the LVDS driver on the DB. The green trace (channel 2) is probing the positive input of the LVDS receiver on the CFB.

Figure 19 compares the positive output of the LVDS driver at the DB to the positive input of the LVDS receiver at the CFB on the opposite end of the cabling. The

[12]The effective electric permittivity in a twisted pair cable is an average of the relative permittivity of air ($\epsilon_r \approx 1.00$) and the relative permittivity of the insulating material [12].

oscilloscope captures in Figure 19 were taken before the FPGA slew rate was changed to fast. In a properly functioning LVDS circuit, the peak-to-peak voltage should be at least 100 mV with a common-mode voltage of 1 V. However, as a result of the slow FPGA slew rate, the peak-to-peak voltage at the LVDS receiver in Figure 19b was 75 mV and the common-mode voltage was likely less than 1 V. This is not sufficient for the LVDS receiver to distinguish between the input high and low voltage thresholds, so it gave the appearance that the system cabling was at fault for bit error rates greater than zero.

OrCAD PSPICE Simulations

The first step in the cable investigation involved simulation to evaluate the likelihood of signal integrity problems being caused by the cabling. OrCAD's schematic capture and PSPICE capabilities were the logical choice. Although an OrCAD library exists for modeling various transmission lines, it was not available. Instead, a lumped element approach was taken based on the three-segment RLCG model. From Figure 20, parameter R is the loop resistance; L is the line inductance; C is the shunt capacitance; and G is the shunt conductance [13, 14]. One segment is labeled ΔX, while the length of the wire is denoted as X. This creates a balanced transmission line model that incorporates physical characteristics of a real cable.

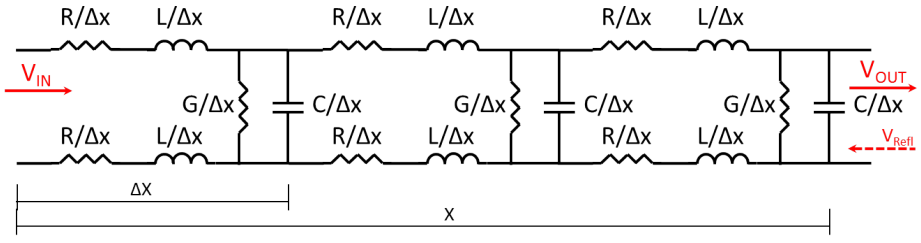


Figure 20: Balanced three-segment RLCG transmission line model.

The DC loop resistance of each twisted pair was determined by shorting together the two wires at one end of the pair, and measuring the resistance of the looped wire with a Fluke 187 digital multimeter. An offset resistance was measured by shorting together the multimeter leads and recording the displayed value. This offset was subtracted from the measured DC loop resistance of each pair; the results are shown in Appendix B. The shunt capacitance was measured between two wires within a pair using an Agilent U1701A capacitance meter. Note that the far end of each pair was left open-circuited during this measurement. The capacitance data for each twisted pair are shown in Appendix B. The average DC loop resistance and average shunt capacitance, 0.6322 Ω and 82.24 pF, were used in the PSPICE schematic shown in Figure 21. The value used for the inductors was calculated using the twisted pair transmission line equations found on page 428 of [12]; these equations and calculations are also shown in Appendix D.

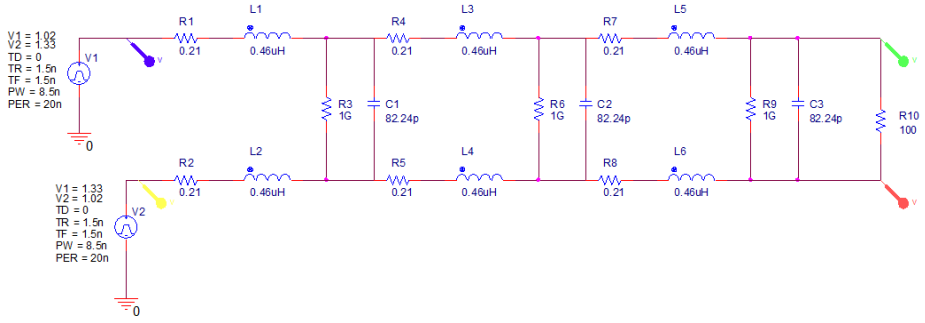


Figure 21: OrCAD schematic of RLCG model using system parameters.

Figure 22 shows the 50 MHz simulation of the system cabling based on the RLCG model. Note that Texas Instruments only provides IBIS models for the parts used in this project. PSPICE does not support IBIS models, and all attempts at converting the IBIS models into PSPICE models failed. Therefore, the LVDS driver outputs were emulated[13] with VPULSE voltage sources in the simulation. The top simulation

[13]Based on the TI SN65LVDS047PW (LVDS driver) datasheet.

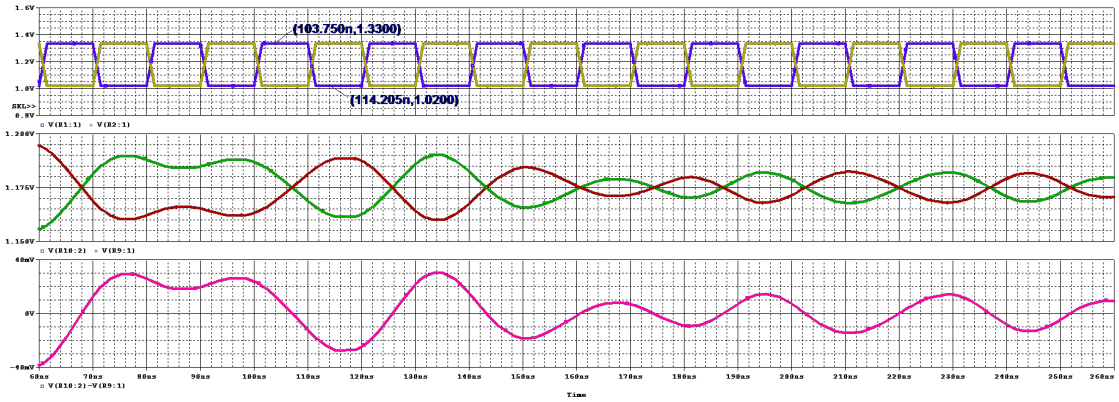


Figure 22: PSPICE simulation of the RLCG twisted pair model at 50 MHz.

plot in Figure 22 shows the LVDS cable input signals with the same characteristics as described in the datasheet for the LVDS driver chip. Specifically, that means rising and falling edge times of 1.5 ns, an output voltage logic high of 1.33 V, and an output voltage logic low of 1.02 V. The middle plot of Figure 22 shows the signal at the far end of the cable where it would normally be received by the LVDS receiver chip. The bottom plot is the difference between the positive and inverted far-end signals.

Based solely on this simulation, it would appear that the cables are reducing the signal quality and causing bit errors. However, there were many assumptions and approximations that were made in order to obtain these results. The simulation did not use a true transmission line model, nor did it use an accurate behavioral model of the LVDS driver chip. Furthermore, the R, L, C, and G parameters in the RLCG model are frequency dependent as noted in [13] and [14]; to keep the model simple, this dependency was disregarded. At best, these results should be considered inconclusive.

Mentor Graphics HyperLynx Simulations

Although HyperLynx is designed for PCB signal integrity simulations, there are ways of manipulating the PCB stackup[14] to emulate various wires, including twisted pair. The twisted pair setup is described in HyperLynx TechNote MG243236 and is provided in Appendix C for convenience. Following these instructions and using the cable parameters calculated in Appendix D, the stackup in Figure 23 was created. Note that each wire's outer diameter (including insulation) was measured with Mitutoyo CD-6CSX calipers and found to be approximately $\varnothing = 40.5$ mil, which agrees with the M22759/11-26 wire specification[15].

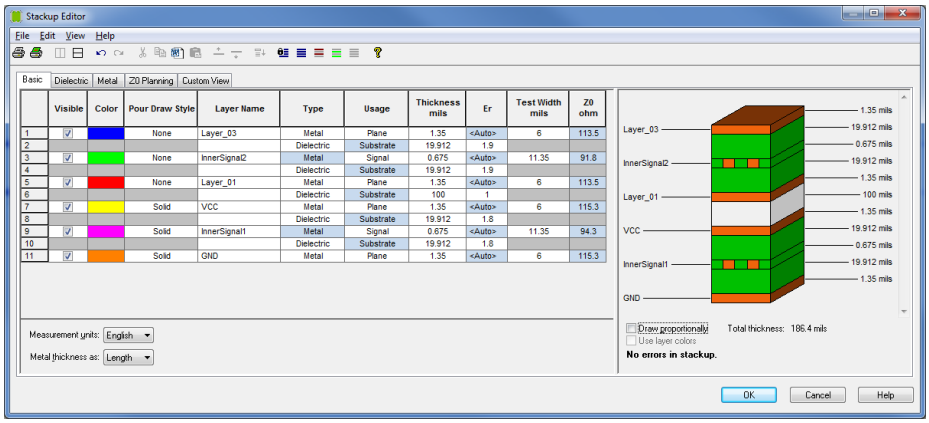


Figure 23: HyperLynx stackup using system cable parameters.

Two transmission lines were configured in series: one representing the warm section of cabling, the other representing the cold section. The warm section is approximately 6 feet in length (pre-twist), while the cold section is approximately 14 inches in length (pre-twist). The HyperLynx LineSim free-form schematic is shown in Figure 24. Note that the impedances shown on the transmission lines (e.g. 115.6 Ω for

[14] In HyperLynx, the stackup contains the mechanical and electrical characteristics of the PCB fabrication process. This includes information such as the dielectric constant and thickness of each FR4 layer; metal type, thickness, and resistivity; and many other properties.

[15] The M22759/11-26 is the military wire specification to which the system cables were manufactured.

the warm cables) are for single-ended signals. However, transmission lines TL3 and TL4 are coupled, as are TL5 and TL6. Thus making their respective differential impedances 167.2 Ω and 134.8 Ω as calculated in Appendix D.

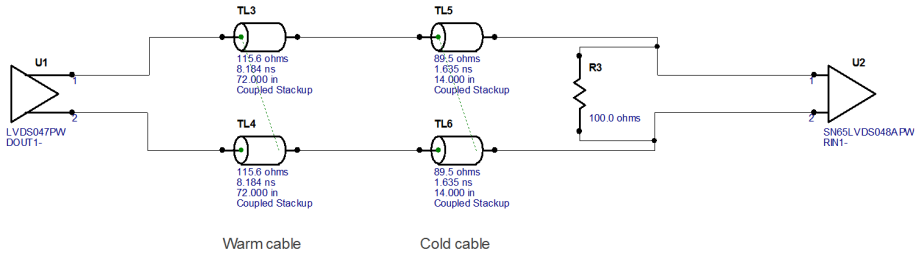
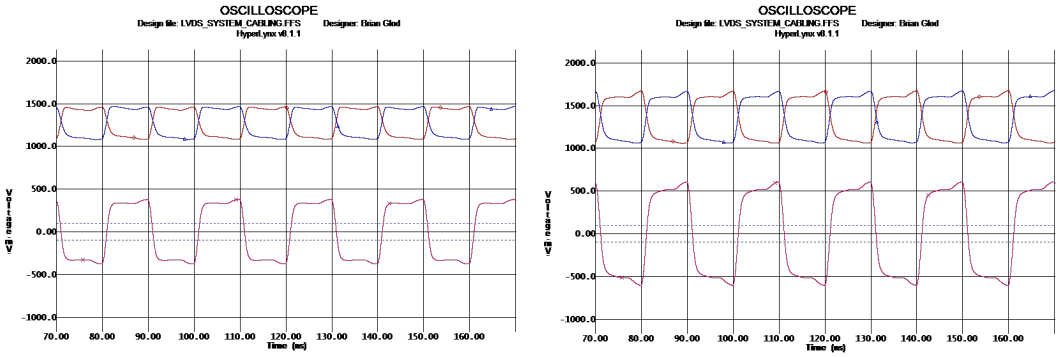


Figure 24: HyperLynx LineSim free-form schematic using system cable parameters.

Before simulating, device models were assigned to the driver and receiver on the transmission line. The driver in this case is the output of a Texas Instruments SN65LVDS047PW chip; and the receiver is the input of a SN65LVDS048APW chip. The models were available in IBIS format from the TI website. The simulation shown in Figure 25a was captured using a 50 MHz stimulus. The top two traces are the LVDS signals sampled at the receiver; the bottom trace is the mathematical difference between the positive and negative LVDS signals. Based on this simulation, the cables appear to be problem-free, which does not agree with the previous PSPICE simulations.

One feature of HyperLynx is its termination wizard, which computes the optimal termination resistance given a transmission line topology. This feature suggested a termination resistance of 161.9 Ω. The corresponding simulation at 50 MHz is shown in Figure 25b. Although the signal quality does not appear to be significantly "better" than the 100 Ω-terminated simulation, it does have a larger magnitude, which could be helpful in certain edge cases.



(a) Termination R = 100 Ω (b) Termination R = 161.9 Ω

Figure 25: HyperLynx LineSim simulation of the system cables at 50 MHz. (a) Shows the resulting waveforms using 100 Ω termination. (b) Shows the resulting waveforms using the optimal termination resistance of 161.9 Ω as calculated by the HyperLynx termination wizard.

4.3 Category 5e Cable Simulations

Because the PSPICE and HyperLynx simulations based on the system cabling were in disagreement, additional simulations were performed using a standard category 5e ethernet cable. Typical category 5e cable is designed to support frequencies beyond 100 MHz at distances of nearly 100 m (328 feet), so it made sense to simulate a cable with this specification to establish a baseline. Furthermore, to rule out the possibility that the cable measurements were invalid, a 25-foot length of category 5e cable was sacrificed and measured using the same methods as the system cables. The cable displayed the following on its sheathing: "GrandMax UTP Cat.5e/350 MHz Patch ISO/IEC 11801 & EN 50288 & TIA/EIA-568-B.2 ETL/3P Verified For Gigabit Ethernet 24 AWG x 4P Type CM(UL) C(UL) CMH E164469-F3 RoHS".

The cable's length was measured and found to be $X = 307.25$ inches. The outer diameter of each wire was measured using Mitutoyo CD-6CSX calipers; all wires had an approximate diameter of $\varnothing = 38.0$ mil.

Because the cable contains twisted pairs, each with a different twist rate, the actual distance traveled by a signal is slightly longer than the measured length of the cable. This distance can be estimated using geometry; specifically, by wrapping a right triangle around a cylinder. Referring to Figure 26, let one of the legs, a, be the circumference of the cylinder (calculated using the measured diameter of the wire including insulation); the other leg, b, is the measured length of a single twist; and the hypotenuse, c, is the distance traveled by the signal in one twist. The length of the hypotenuse can be determined using the Pythagorean Theorem, shown in Equation 3.

$$c = \sqrt{a^2 + b^2} = \sqrt{(\pi \varnothing)^2 + b^2} \tag{3}$$

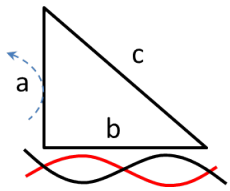


Figure 26: Diagram of right triangle, labeled according to Equation 3.

The length per twist (b) was measured and recorded in Table 2. Also shown in Table 2 is the computed length of wire per twist (c from Equation 3), and the one-way distance traveled by the signal as computed by Equation 4.

$$\text{total distance traveled} = X \cdot \left(\frac{c}{b}\right) \tag{4}$$

The electrical measurements are listed in Table 3. Resistances were measured with a Fluke 187 digital multimeter, the capacitances were measured with an Agilent U1701A capacitance meter, and the inductances were calculated using Equation D.3. Note that the inductance was calculated with an estimated wire separation equal to the outer diameter of one wire, or 38 mil.

Table 2: Measured cat. 5e twist rates

Pair color	Twist Length (b, inch)	Length of wire per twist (c, inch)	Distance traveled (Eq. 4, inch)
Orange	0.7110	0.7210	311.55
Green	0.6010	0.6127	313.25
Blue	0.5660	0.5785	314.01
Brown	0.7930	0.8019	310.71
Average	-	-	312.66

Table 3: Measured/calculated cat. 5e electrical parameters

Pair color	Measured DC Loop Resistance (Ω)	Measured Capacitance (pF)	Calculated Inductance (µH)
Orange	1.51	381.5	3.756
Green	1.62	384.5	3.776
Blue	1.87	392.2	3.786
Brown	1.41	386.1	3.746
Average	1.602	386.08	3.766
Std. Dev.	0.198	4.507	0.0158

OrCAD PSPICE Simulations

Using the average RCL and length values from Tables 2 and 3, the OrCAD PSPICE RLCG schematic in Figure 27 was simulated. Figure 28 shows the 50 MHz simulation of the category 5e cable using the same signal parameters used previously in Figure 21. Initially, the waveforms at the receiver end of the cable (middle and bottom plots of Figure 28) appear to be in excellent condition—there is no noise, ringing, or other abnormal oscillation patterns that were observed in Figure 22. However, upon further inspection, it becomes apparent that there is a flaw in the simulation. The signal at the receiver end of the cable has a frequency of about 15 MHz, yet the input signal is 50 MHz. Because of this near impossibility, the PSPICE results for the RLCG lumped model of a transmission line should be considered unreliable. As in

the PSPICE simulations of the system cabling, this inaccuracy is most likely because of the many assumptions and estimations that were made in the schematic model.

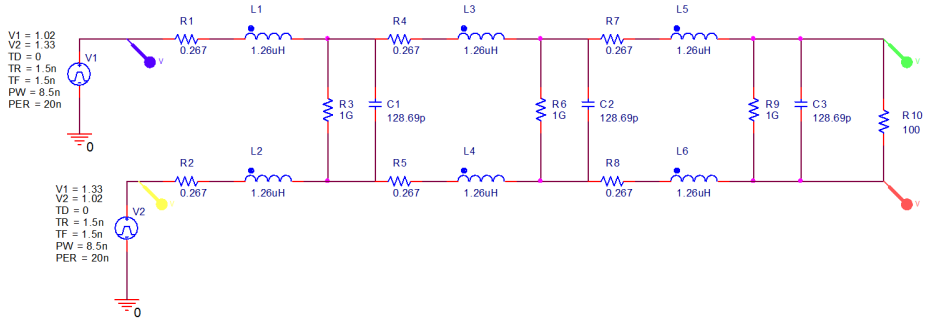


Figure 27: OrCAD schematic of RLCG model using category 5e cable parameters.

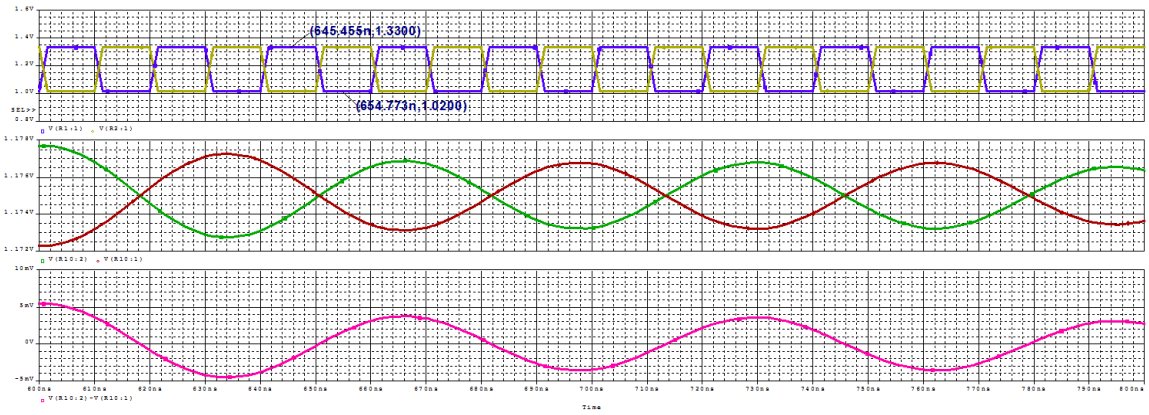
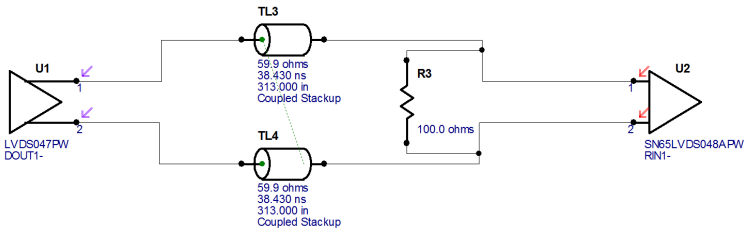


Figure 28: PSPICE simulation of the RLCG category 5e model at 50 MHz.

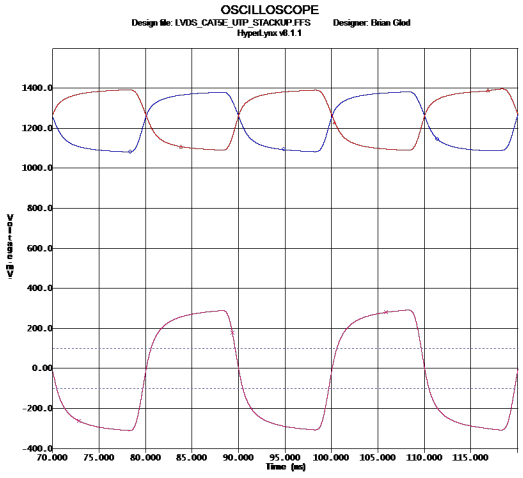
Mentor Graphics HyperLynx Simulations

Because of the seemingly impossible PSPICE simulation results, the category 5e cable simulations were repeated using HyperLynx LineSim following the twisted pair stackup instructions in Appendix C. The LineSim schematic is shown in Figure 29a, while the 50 MHz simulation is shown in Figure 29b. The HyperLynx results show a nearly perfect signal along the length of the simulated category 5e cable. The peak-to-peak voltage of the LVDS signal at the receiving end is well above the minimum

requirement of 100 mV, and there is no ringing or other noise on the waveforms. Furthermore, the frequency of the driving signal did not change as the signal traversed the cable, which is what is supposed to happen. Since HyperLynx uses real transmission line models and supports IBIS models for the LVDS driver and receiver, and the results were not absurd, it is reasonable to conclude that the HyperLynx results are more trustworthy than the PSPICE results.



(a) LineSim free-form schematic of cat. 5e cable



(b) Simulation of cat. 5e at 50 MHz

Figure 29: HyperLynx LineSim free-form schematic and simulation of cat. 5e cable.

4.4 The LVDS and TDR Test Board

Although the HyperLynx simulations of the system cables and the category 5e cable were reasonable, they did not match the severely degraded signals observed on the oscilloscope in Figure 19. To eliminate all doubt about the performance of the sys-

tem cabling, a combination time-domain reflectometer (TDR)/LVDS test PCB was designed. The test board, shown in Figure 30, was designed around the same components used in the imaging system electronics. This allows for testing of standardized UTP such as category 5e ethernet cable, as well as individual pairs of the system cabling while maintaining a close relation to the real system. The relevant components include: two TI SN65LVDS047PW LVDS drivers, two TI SN65LVDS048APW LVDS receivers, and one TI SN74LVC16244A-DGG buffer. Power is sourced with a 5 V wall-wart supply, which is fed into a National Semiconductor (now TI) LP3873ES-3.3 linear regulator to produce the 3.3 V supply necessary for the components on the board.

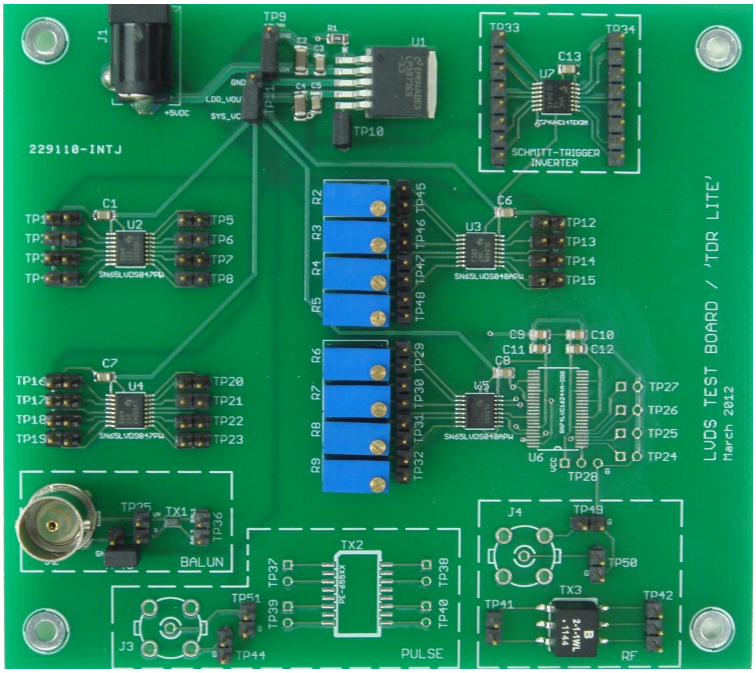


Figure 30: LVDS test board with TDR capabilities.

Another feature that was incorporated into the LVDS test board is a rudimentary TDR specifically for balanced transmission lines. The TDR is an excellent way of measuring signal reflections that may be occurring due to improper termination.

Trimmer potentiometers may be used for tuning the termination resistance to minimize signal reflections. A properly tuned terminator eliminates signal reflections, and its value is equal to the characteristic impedance of the cable. More details about the design and operation of the TDR/LVDS Test Board are in Appendix E.

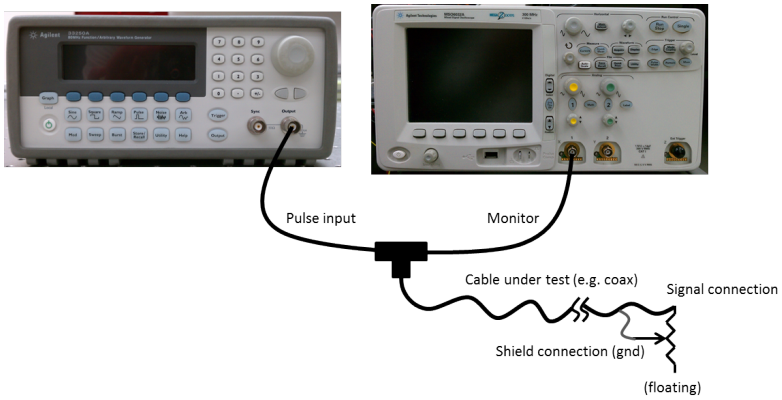


Figure 31: A single-ended TDR constructed with common lab equipment.

A very basic TDR can be constructed with ordinary laboratory equipment; all that is required are a signal/pulse generator, an oscilloscope, and the cable under test. This setup is shown in Figure 31 and is accurate when compared to a professional TDR instrument. However, testing a balanced transmission line, such as twisted pair, requires a slightly different setup in order to produce accurate results. One method is to use a signal generator that features differential outputs and an oscilloscope with a differential probe. Neither of these instruments were available to CfD, so an alternative method using a balun transformer was implemented on the LVDS test board[16]. The balun transformer is a passive component that converts a single-ended (UNbalanced) signal to a differential (BALanced) signal that can be launched over a balanced transmission line. Any reflections are converted back to single-ended for observation on the oscilloscope.

[16]This is not a novel idea, it is discussed in [14].

The key characteristics of the pulse generator used in a TDR are the rise and fall times. Faster edge times provide better resolution. This is more important for testing shorter-length cables since longer edge times may obscure reflected pulses. The signal generator used in this setup is an Agilent 33250A, which has a minimum pulse edge time of 5 ns and a minimum square wave edge time of 8 ns. Therefore, the test board was designed with a Toshiba TC74VHC14TEK2M hex Schmitt-trigger inverter as a simple way to help reduce these edge times.

Schmitt-trigger Functionality Test

One of the first features tested on the LVDS Test Board was the Schmitt-trigger inverter. In this test, the signal generator was configured to output a 0 V to 3.3 V square wave at 1 MHz with a 50 Ω impedance. The output from the signal generator was fed to the "1A" input of the Toshiba Schmitt-trigger inverter, and the "1Y" output was monitored on the oscilloscope. Figure 32 shows that the Schmitt-trigger inverter reduced the edge times from approximately 7 ns (measured from 5% to 95%) to approximately 3 ns.

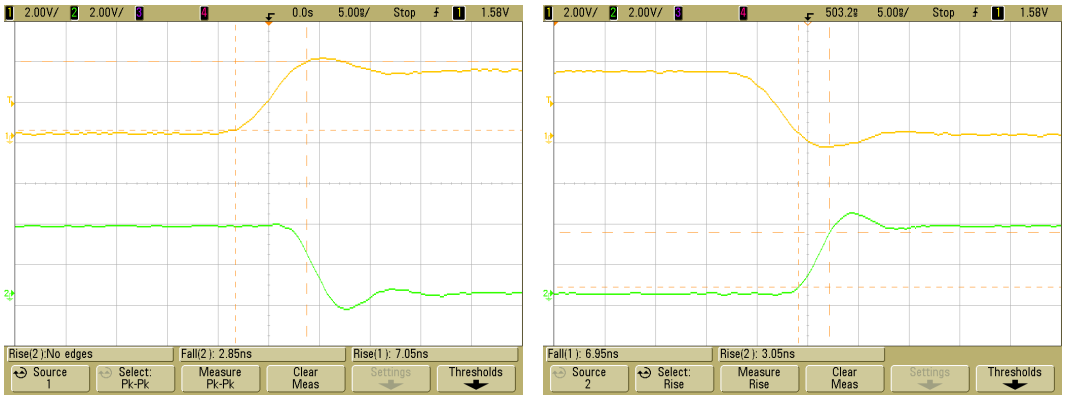


Figure 32: Oscilloscope capture demonstrating the effects of a Schmitt-trigger on edge times. Channel 1 (yellow) is the input, and channel 2 (green) is the output.

Balun TDR Results: Category 5e Cable

The connection diagram for this test using category 5e cable is shown in Figure 33. Figure 34 shows the bench setup using the LVDS/TDR Test Board.

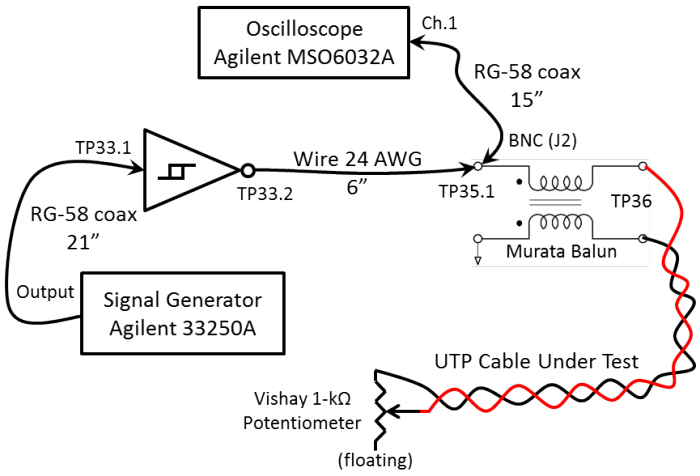


Figure 33: Balun TDR connection diagram.

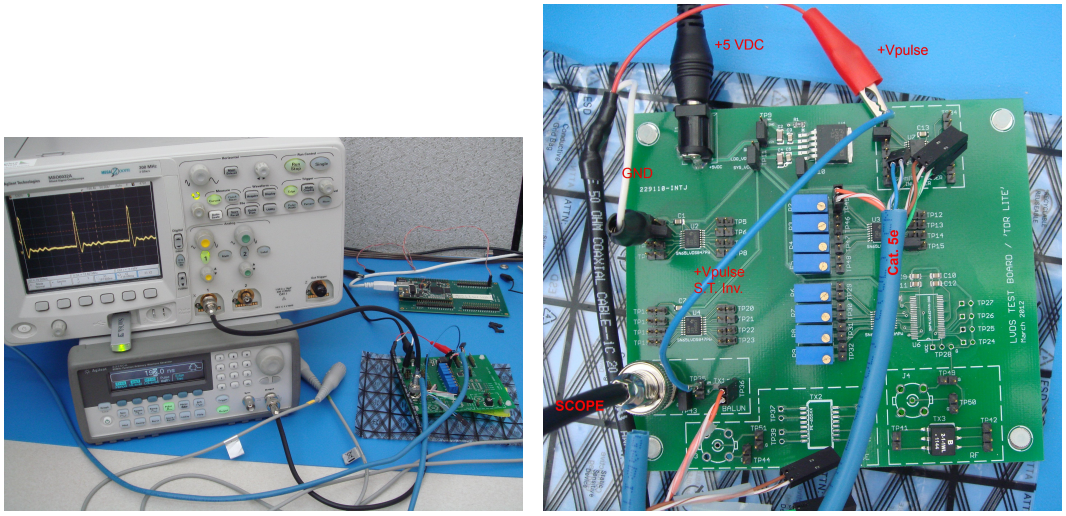
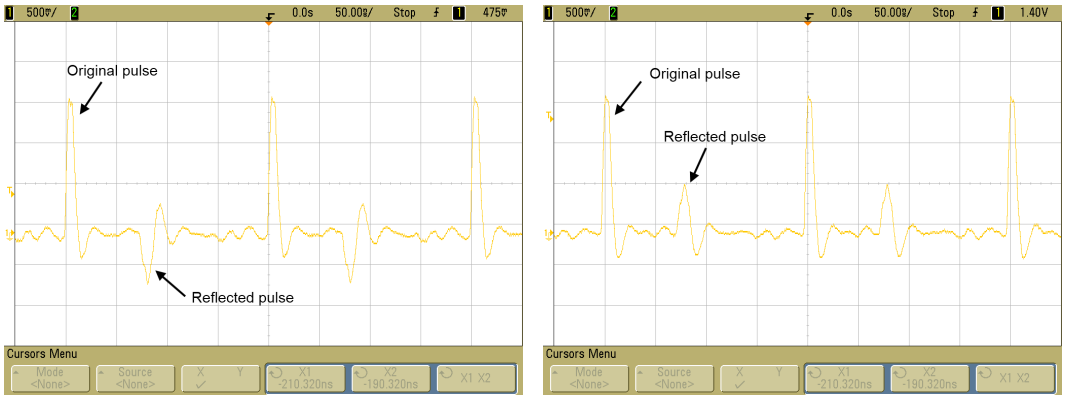


Figure 34: Bench setup of balun TDR.

When in the TDR configuration, the Agilent 33250A signal generator was programmed to output a 5 MHz, 0 V to 3.3 V pulse of width 192 ns. The pulse entering

the cable is inverted, so it corresponds to an 8 ns pulse width at 3.3 V; the Schmitt-trigger inverter reduces the edge time to approximately 3 ns. Figure 35 shows the effects of mismatched termination on the cat. 5e cable, which is designed for 100 Ω termination. The large pulse is the original pulse created by the signal generator. The smaller pulse roughly 78 ns after the initial pulse is the reflection caused by the mismatched termination.



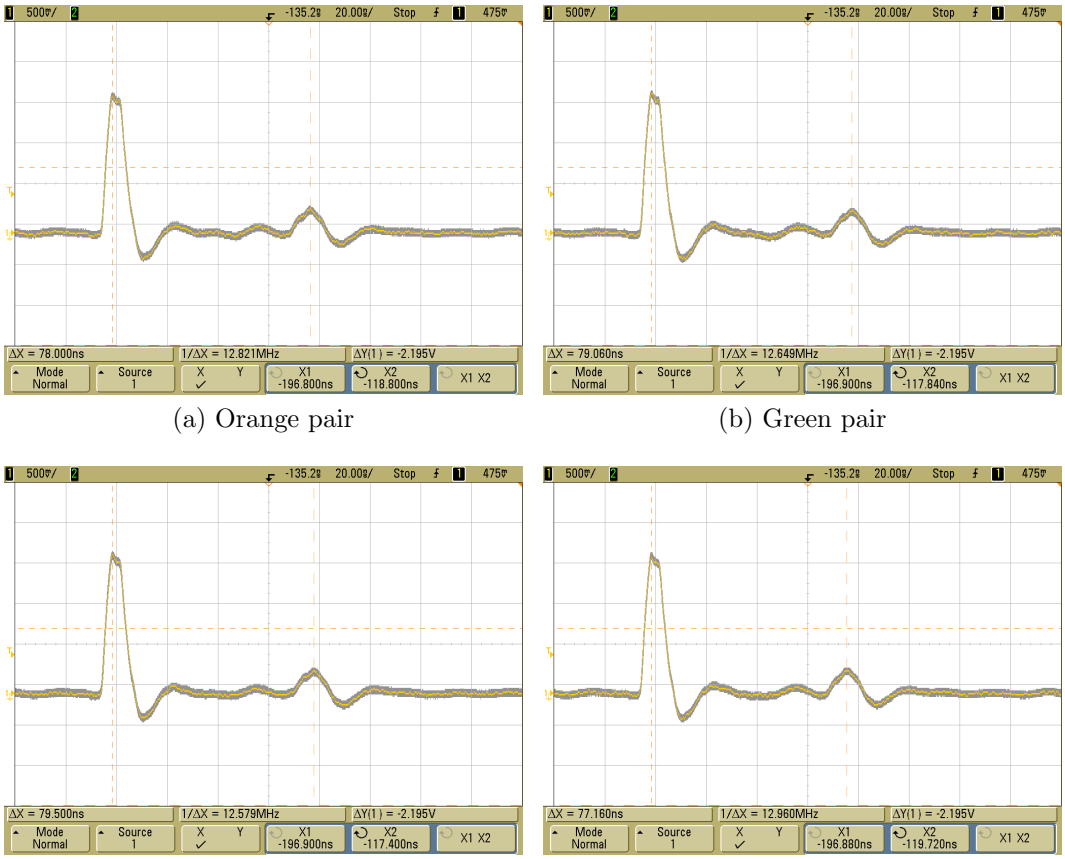
(a) Termination is 19.26 Ω (b) Termination is 362.14 Ω

Figure 35: Effects of mismatched termination on cat. 5e cable. The optimal termination for cat. 5e is 100 Ω.

Using the potentiometer to tune the termination and minimize the reflected pulse, a lower and upper bound was established at 91.8 Ω and 107.9 Ω, respectively. Averaging these resistances produces 99.85 Ω, which is within 0.15% of the optimal value of 100 Ω.

Because the oscilloscope captures the original pulse and the reflected pulse on a time axis, the length of the cable can be measured using the Round-Trip Time (RTT)[17]. The RTT is equal to the time difference between the original pulse and the reflection; the one-way time is half of this. The oscilloscope captures shown in Figure 36 display the RTT of each pair within the cat. 5e cable.

[17]In this manner, TDRs can be used to determine the location of an impedance discontinuity (e.g. broken, damaged, or water-saturated cable) in a long run of cable that may not easily be accessible.



(a) Orange pair (b) Green pair

(c) Blue pair (d) Brown pair

Figure 36: Round-Trip Time measurement of cat. 5e using TDR.

$$\text{length} = \frac{\text{RTT}/2}{(84.72 \times 10^{-12}) \cdot \sqrt{\epsilon_{r,eff}}} \tag{5}$$

The RTTs from Figure 36 and calculated RTT/2 are shown in Table 4. Using this data, the length of the cable can be established using the characteristics of the cable and Equation 5. However, the particular cat. 5e cable used in this experiment does not have markings indicating the wire insulation material, which strongly impacts the $\epsilon_{r,eff}$ value. The exact insulation material is not part of the TIA/EIA-568-B specification—it can be any thermoplastic. Typical materials are polyethylene (PE, $\epsilon_r = 2.25$), polyvinyl chloride (PVC, $\epsilon_r = 3.0$), and Teflon (PTFE, $\epsilon_r = 2.1$).

Using an estimated wire separation equal to the diameter of a single wire (38 mil), Teflon gives a characteristic impedance closest to $100\,\Omega$ ($\approx 98\,\Omega$), but PE is cheaper and thus much more common than Teflon. It is also important to recall that $\epsilon_{r,eff}$ is *some* average between the ϵ_r of the wire insulation material and the ϵ_r of air. Thus, $\epsilon_{r,eff}$ depends on the wire spacing and will be slightly less than the ϵ_r of the insulation material itself.

$$\epsilon_{r,eff} = \left(\frac{D}{s}\right)\epsilon_{r,ins.} + \left(\frac{s-D}{s}\right)\epsilon_{r,air} \tag{6}$$

Equation 6 shows the calculation of the effective relative permittivity based on the outer wire diameter including insulation (D), the wire separation (s), the relative permittivity of the wire insulation material ($\epsilon_{r,ins.}$), and the relative permittivity of air ($\epsilon_{r,air} \approx 1.00$).

Attempting to solve Equation 5 for the wire length is somewhat counterproductive since it is very sensitive to changes in $\epsilon_{r,eff}$, which is based on two unknowns/estimations: the separation between the wires, and the relative permittivity of the insulating material. Instead, the calculated wire length is perhaps the most accurate of the available variables. Thus, rearranging Equation 5 and solving for the effective relative permittivity yields the right-most column of Table 4, which strongly suggests the insulating material is PE. From these calculations, it is evident that TDR measurements can reveal significant information about a cable's electrical parameters. However, for applications requiring fast and accurate cable parameters, the use of specialized equipment such as a network analyzer is preferred.

Table 4: Measured cat. 5e Round-Trip Times and calculated $\epsilon_{r,eff}$

Pair color	Measured RTT (ns)	Calculated RTT/2 (ns)	Calculated Length (in.) (Equation 4)	Calculated $\epsilon_{r,eff}$ (Equation 5)
Orange	78.000	39.00	311.55	2.183
Green	79.060	39.53	313.25	2.219
Blue	79.500	39.75	314.01	2.233
Brown	77.160	38.58	310.71	2.148

Balun TDR Results: System Cables

The system cables were connected to the TDR in order to check for signal reflections and to tune the potentiometer to establish the proper termination resistance. The oscilloscope used during these tests was an Agilent InfiniiVision 7054A[18] with an Agilent N2795A 1 GHz active probe. Figure 37 shows the TDR waveform when the twisted pair carrying the FPGA_CLKIN signal is terminated with resistor R24 on the CFB. Resistor R24 was measured with the Fluke 187 multimeter and found to be 100.14 Ω. It is clear from Figure 37 that no reflections exist, indicating that the 100 Ω termination resistors are adequate.

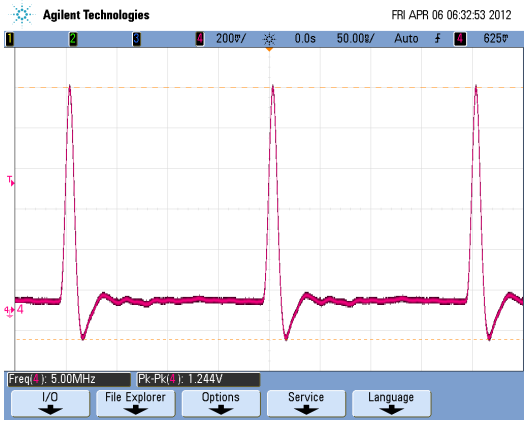
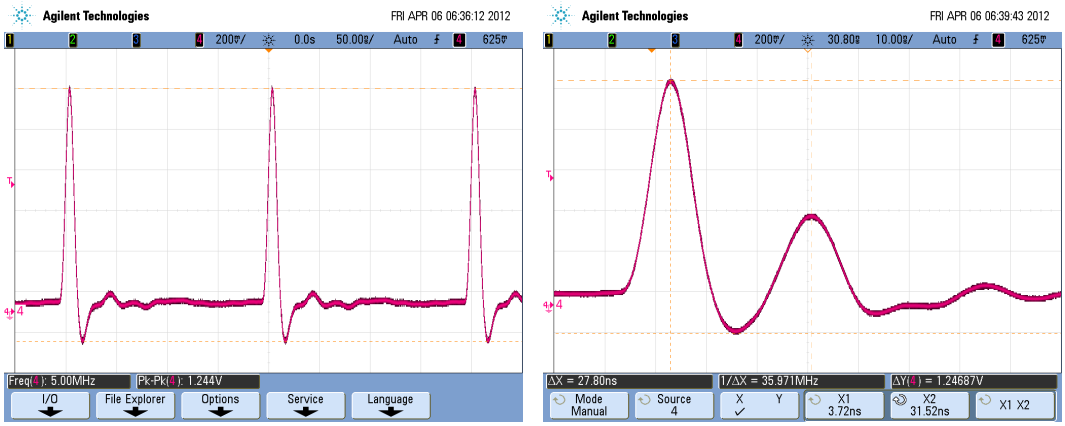


Figure 37: Balun TDR of FPGA_CLKIN terminated at R24 on the CFB.

[18]This oscilloscope features four channels, 500 MHz of bandwidth, and a sample rate of 4 GS/s.

The TDR measurements were repeated with the FPGA_CLKIN twisted pair, but terminated at one of the potentiometers on the LVDS/TDR Test Board. Figure 38 compares the correct termination ($R = 100.23\,\Omega$) with severe termination mismatch when $R = 492.4\,\Omega$.



(a) Termination is $100.23\,\Omega$ (b) Termination is $492.4\,\Omega$

Figure 38: The oscilloscope capture in (a) shows no signal reflections, indicating proper termination; (b) shows a reflected pulse nearly 28 ns after the primary pulse. The reflection occurs because the termination resistance is not equal to the characteristic impedance of the cable.

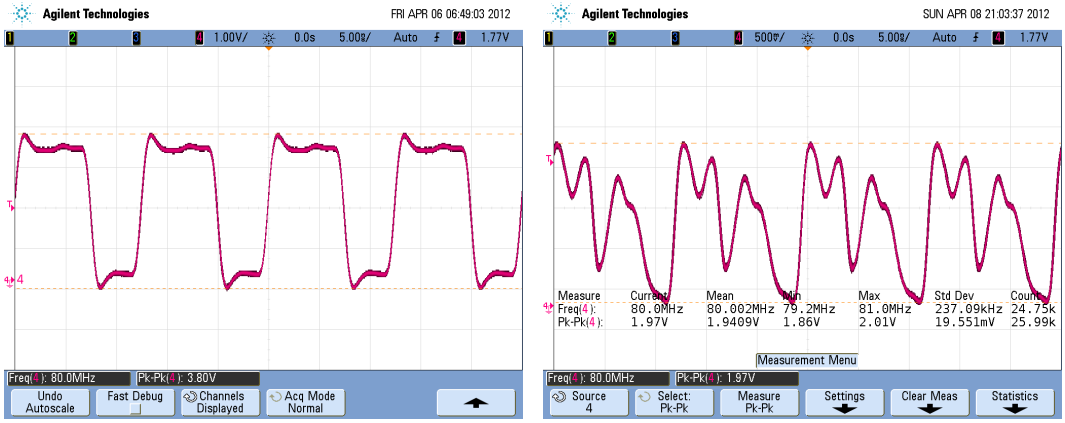
From Figure 38b, the RTT of FPGA_CLKIN is approximately 27.80 ns, which can be used to determine the cable length if desired. However, the spacing between the wires in the pair is not uniform, and calculating the exact cable length is not necessary at this time.

LVDS Test Results: System Cables

The LVDS drivers and receivers were tested using the LVDS/TDR Test Board and compared with the results from the CFB, shown in Figure 39. The Agilent 33250A signal generator was configured to output an 80 MHz square wave from 0 V to 3.3 V. This signal entered the LVDS/TDR Test Board at the "1A" input of the Schmitt-

trigger inverter; the "1Y" output was connected to the "DIN4" input of the LVDS driver. The corresponding LVDS output was connected to the FPGA_CLKIN pair of the system warm cable, which passed through the dewar flange to the cold cable.

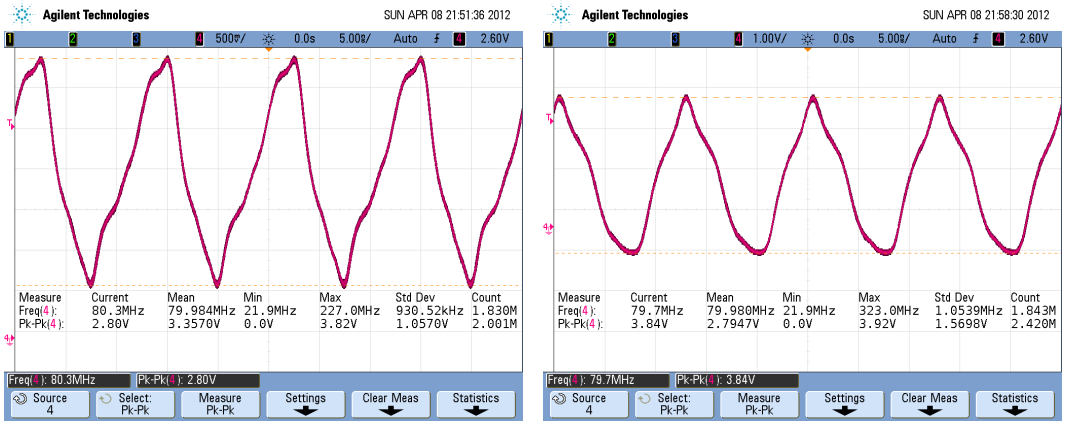
In Figure 39a, the FPGA_CLKIN pair on the cold cable was terminated at potentiometer R5 on the Test Board. The signal entered the LVDS receiver, and the single-ended output was probed with the oscilloscope. In Figure 39b, the cold cable was connected to the CFB via connector J2 where the FPGA_CLKIN pair was terminated, and the single-ended output of LVDS receiver U63 was probed at TP17.



(a) Terminated at LVDS Test Board (b) Terminated at CFB

Figure 39: The output of the LVDS receiver when the input (FPGA_CLKIN) is terminated on (a) the LVDS/TDR Test Board with $R_{term} = 100.23\,\Omega$; and (b) the CFB with $R_{term} = 100.14\,\Omega$.

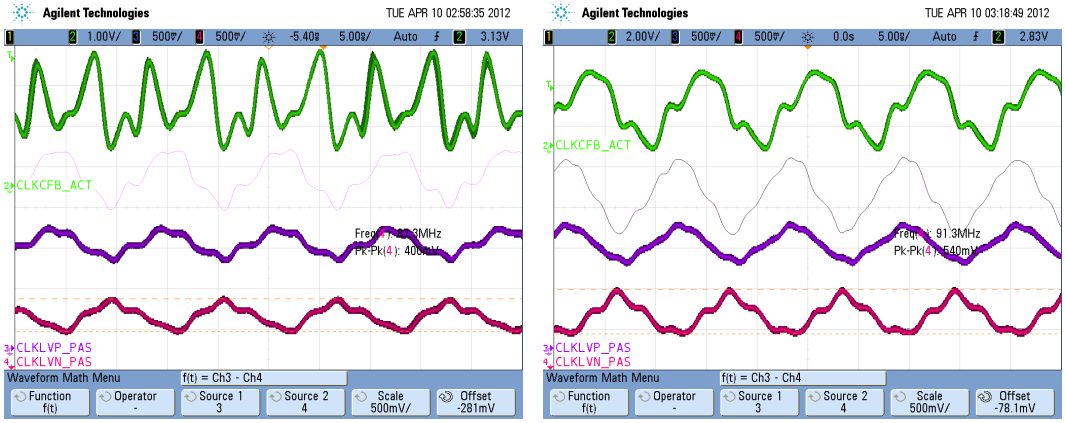
Figures 39 and 40 reveal major flaws on the Cold Fanout Board, particularly on the FPGA_CLKIN signal path. To observe the signal behavior during normal system operation, the warm cables were reconnected to the DB, and a 90 MHz clock signal was generated by the XEM3010 on the WEB. Figure 41 compares the resulting FPGA_CLKIN and PDRST_GBL signals on the CFB. The positive and inverted LVDS signals were also sampled using Agilent 10073C passive probes. The LVDS input signals on both paths have a similar shape and minor noise/ringback is evi-



(a) FPGA_DIN0 (b) CDPCHG_IN

Figure 40: The output of the LVDS receiver when the input is terminated on the CFB. (a) Shows the FPGA_DIN0 signal, and (b) shows the CDPCHG_IN signal. Although not square waves, neither (a) nor (b) exhibit excessive ringback and are therefore superior to FPGA_CLKIN.

dent. While both LVDS output signals are less than ideal, FPGA_CLKIN is highly unusable—its effective clock rate is nearly 180 MHz. This suggests the FPGA_CLKIN signal path on the CFB has a design flaw on the output of LVDS receiver U63.



(a) FPGA_CLKIN (b) PDRST_GBL

Figure 41: Comparison of a 90 MHz signal over the FPGA_CLKIN and PDRST_GBL signal paths terminated on the CFB. Channel 2 (green) is the active probe at the LVDS receiver output. Channel 3 (purple) and channel 4 (pink) show the inputs to the LVDS receiver. The math function shows the difference between channels 3 and 4.

4.5 HyperLynx Simulations of the Cold Fanout Board

The schematic capture and manual layout of the 6-layer CFB was performed using Cadsoft Eagle PCB version 5.11. The design was not specifically optimized for differential pair signaling, nor was it optimized for high frequency signals. During the initial design phase, it was determined that these considerations would not be necessary for the frequencies that the system would be operating. Furthermore, at the time of layout, the Center for Detectors was unaware that RIT had a license for Mentor Graphics PADS PCB layout tools. If this had been known, the CFB would likely have been designed, or at least simulated, with the Mentor Graphics tools prior to fabrication.

Eagle PCB has many features, including an engine that interprets and runs User Language Programs, or ULPs. The programs allow users to extend the functionality of Eagle and export data for use in other programs. One of the ULPs that comes bundled with Eagle allows users to export the board design to a HyperLynx BoardSim (.hyp) file. The program is named "hyperlynx.ulp" and is found in the "ulp" directory of the Eagle installation directory. This file can be edited to reflect the manufacturing specifications of the board house. The CFB was manufactured by Sierra Circuits' no-touch ProtoExpress service; the default values in the hyperlynx.ulp program were acceptable and were left unchanged[19]. The exported HyperLynx BoardSim with the FPGA_CLKIN signal path highlighted is shown in Figure 42. The red traces are on the top copper layer; the blue traces are on internal copper layer 4; and the light blue traces are on the bottom copper layer.

[19]The default characteristics were: $\epsilon_{r,FR4} = 4.8$, outer layer copper thickness of 1 oz, inner layer copper thickness of 0.5 oz, and total board thickness of 62.5 mil. The specifications given by Sierra Circuits is similar, except they do not specify $\epsilon_{r,FR4}$.

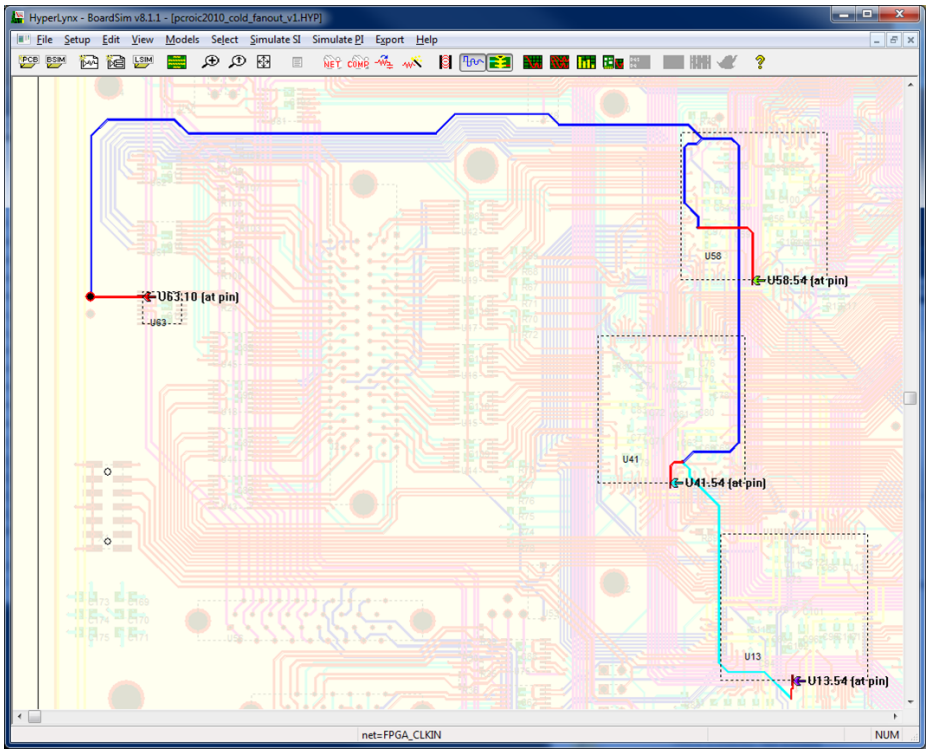


Figure 42: Section of the Cold Fanout Board layout imported into HyperLynx BoardSim. The highlighted net is FPGA_CLKIN, which carries the shared clock signal for the three cold FPGAs. Device U63.10 is the output of the LVDS receiver; devices U13.54, U41.54, and U58.54 are the FPGA clock input pins.

When the BoardSim file is initially opened, the Stackup Verifier displays the message: "WARNING: Layer Bottom is buried and contains components!". The Stackup Verifier also shows that several dielectric layers were added. Attempting to view the stackup information within HyperLynx displays a generic "improper argument" error message, and opening the stackup file in a text editor did not reveal any obvious problems. Directly running a simulation at this point resulted in an error.

Fortunately, HyperLynx allows the designer to select signal paths (nets) within BoardSim and export them as a LineSim free-form schematic, shown in Figure 43. This process also exports the stackup information, which appeared to fix the stackup

errors. The original LineSim stackup information is shown in Figure 44; and the meaning of the BoardSim warning message becomes immediately obvious.

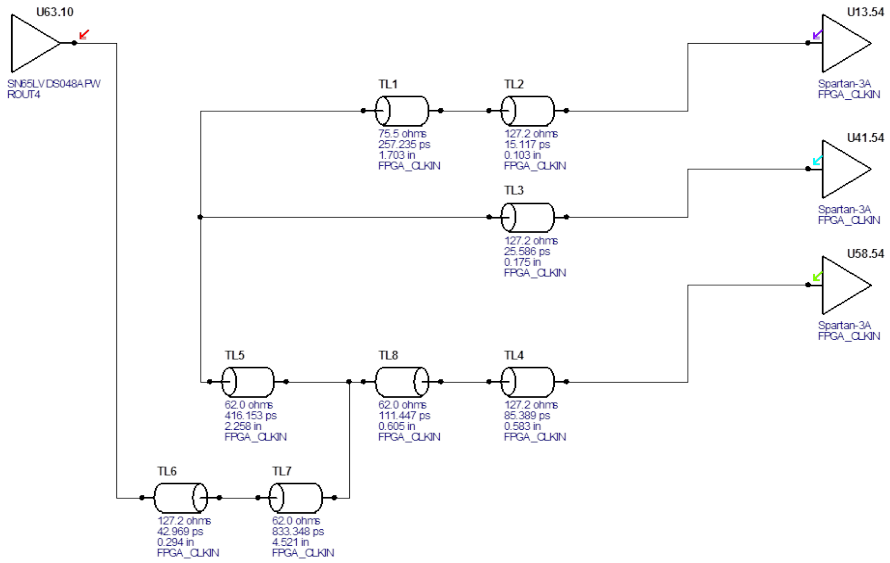


Figure 43: HyperLynx LineSim free-form schematic of FPGA_CLKIN.

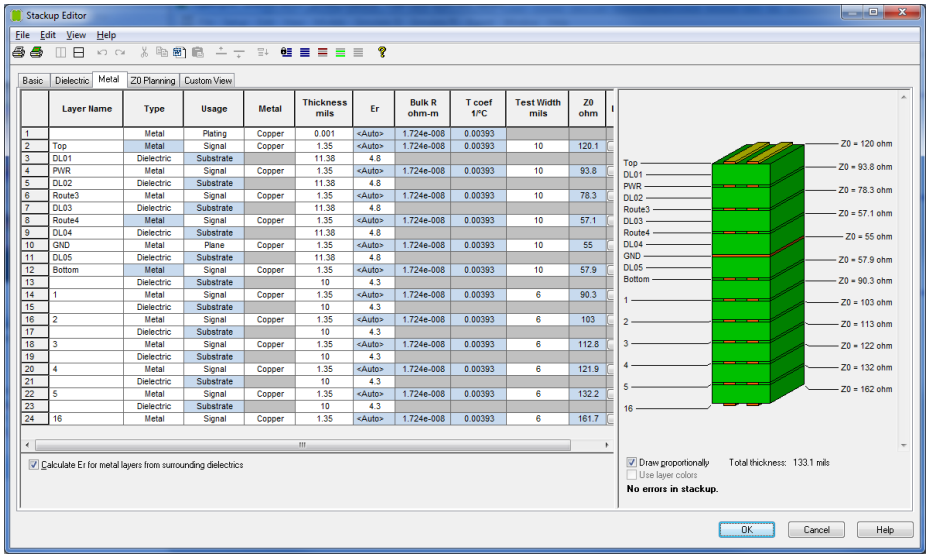


Figure 44: The original HyperLynx LineSim stackup of the CFB. Note that the layer named “Bottom” (which contains components) is buried by the additional layers that were inserted by BoardSim.

The original stackup appeared to have the correct FR4 characteristics, but the inner layer copper thicknesses were 1.35 mil (1 oz) instead of the 0.675 mil (0.5 oz) as specified in hyperlynx.ulp. Additionally, the stackup had extra layers (rows 13 through 24 in Figure 44) that were likely added by the initial stackup verification process performed by BoardSim. The extra layers were removed and the inner layer copper thickness was adjusted; this brought the total board thickness close to the manufacturer's specification of 62 mil. The corrected stackup is shown in Figure 45.

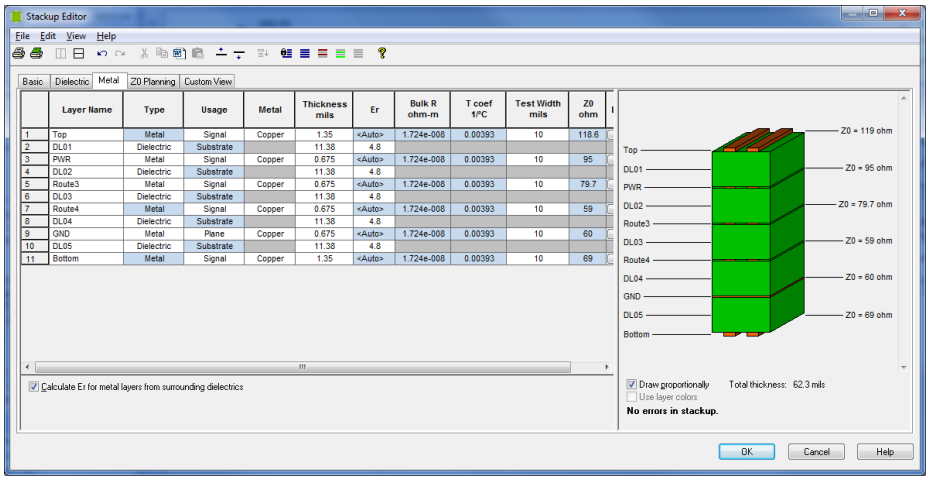


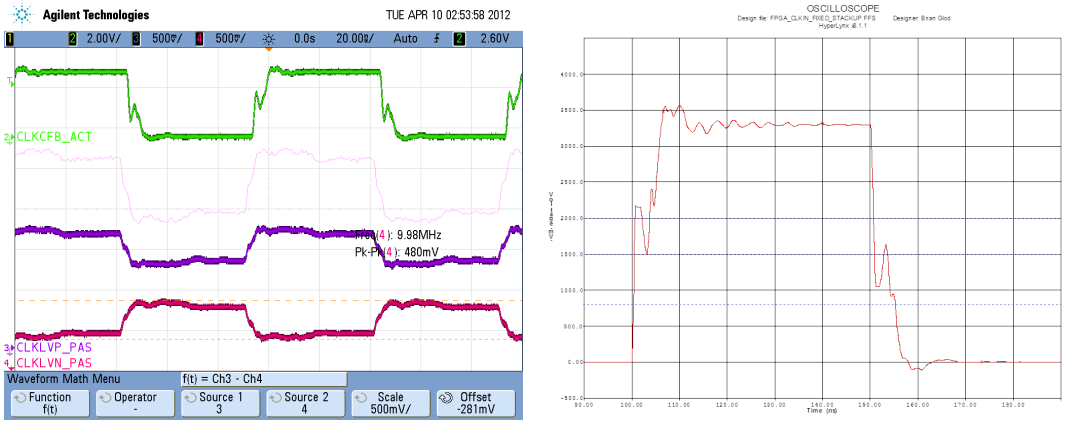
Figure 45: The fixed HyperLynx LineSim stackup of the CFB. Note the proper number of layers, layer thicknesses, and total board thickness.

Before simulating, device models were assigned to the driver and receivers on the transmission line. The driver on the FPGA_CLKIN net is the output of a Texas Instruments SN65LVDS048APW LVDS receiver. The IBIS model for this part was obtained from the TI website. The receivers on the FPGA_CLKIN net are three Xilinx Spartan-3AN FPGAs. The models for these parts were generated using Xilinx ISE[20]. The IBIS models generated by Xilinx ISE are based on the actual design being implemented on the FPGA, which is helpful to ensure accurate simulations.

[20]This is accomplished in the "Processes" section of the "Design" tab. Expand "Implement Design", then "Place & Route", then run "Generate IBIS Model".

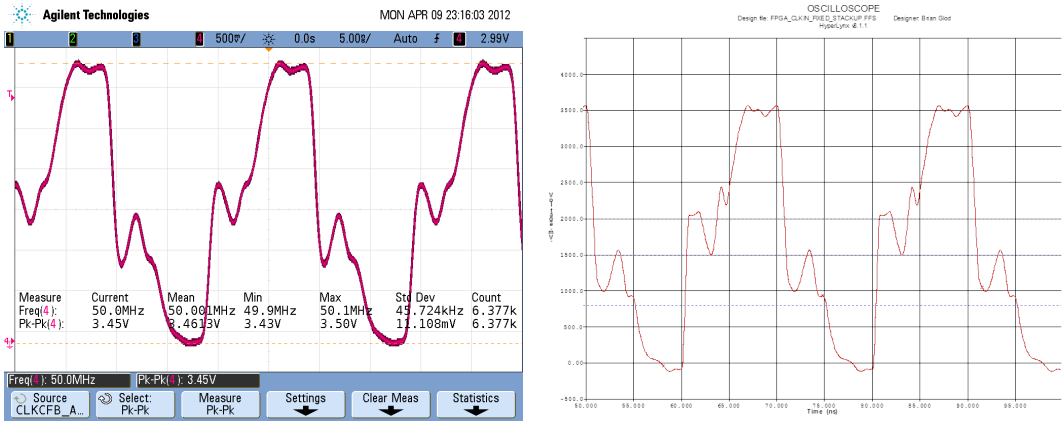
Simulation Results

The FPGA_CLKIN net was simulated at a few frequencies of interest: 10 MHz, 50 MHz, and 80 MHz. The simulated results were compared to the waveforms physically captured with an Agilent InfiniiVision 7054A oscilloscope and were found to be markedly similar, as shown in Figures 46–48.



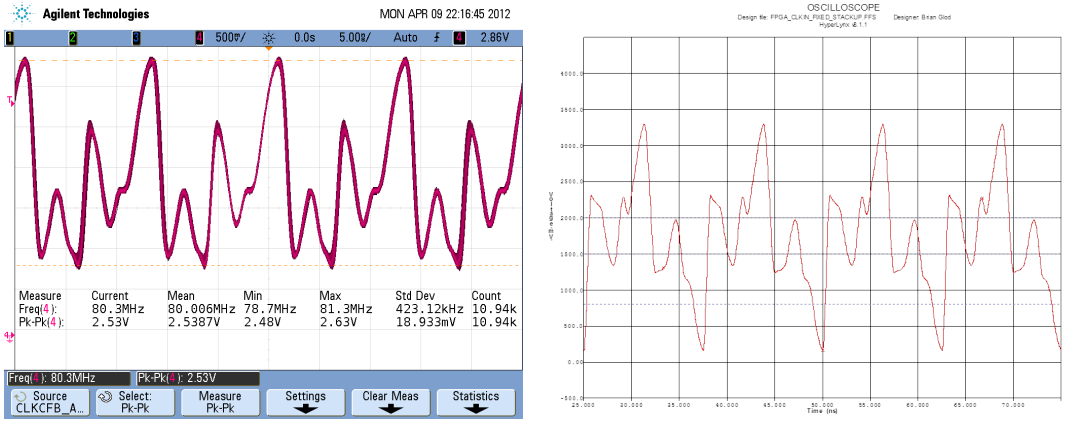
(a) Oscilloscope at TP17 (b) Simulated waveform at U63 pin 10

Figure 46: Comparison of a 10 MHz clock signal on FPGA_CLKIN.



(a) Oscilloscope at TP17 (b) Simulated waveform at U63 pin 10

Figure 47: Comparison of a 50 MHz clock signal on FPGA_CLKIN.

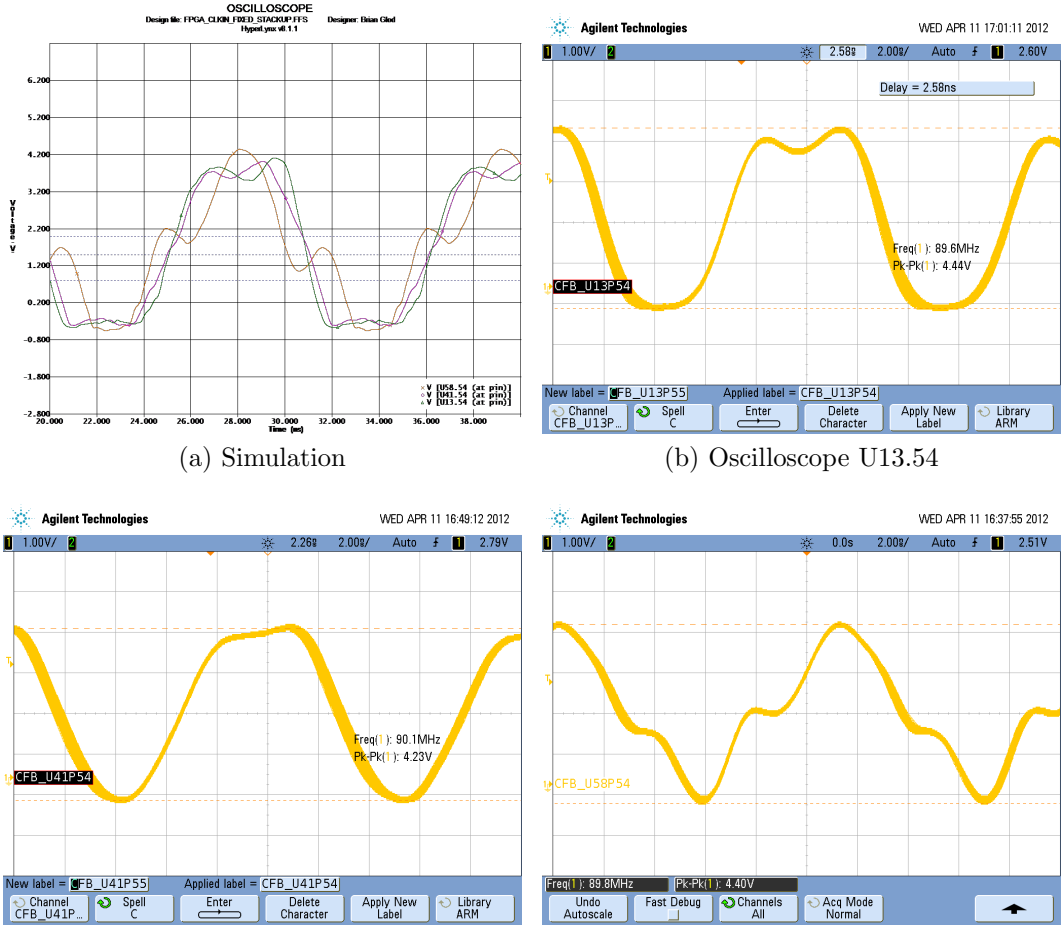


(a) Oscilloscope at TP17 (b) Simulated waveform at U63 pin 10

Figure 48: Comparison of a 80 MHz clock signal on FPGA_CLKIN.

The BER results demonstrate that FPGA U58 was consistently the first to fail. As the frequency continued to increase, U13 would follow and U41 was the last to fail. The HyperLynx simulations also recorded the signal waveforms as they appeared at the clock input (pin 54) of each FPGA. Figure 49 compares the 90 MHz simulated FPGA_CLKIN signal at each FPGA clock input to the waveform captured at the same points using an Agilent MSO6032A oscilloscope. The consolidated simulation plot in Figure 49a clearly shows that U58 (orange) exhibits some ringback[21] on the rising and falling edges. Ringback can be acceptable on some clock nets provided the setup and hold times of the device are met [15]. For the case of the Spartan-3AN FPGA, the setup time is 2.12 ns and the hold time is 100 ps as per the datasheet. Although somewhat difficult to discern from the U58 plots (Figures 49a and 49d), the setup timing requirement does not appear to be met. It is interesting to note, however, that the U13 waveforms do not appear to have obvious signal integrity problems despite a 21% BER failure rate at 90 MHz. By comparison, U58 and U41 have 100% and 0% failure rates, respectively.

[21] Ringback is when a signal crosses the input high voltage (or input low voltage) and re-crosses the threshold again before finally settling above V_{IH} (or below V_{IL}) [15].



(a) Simulation

(b) Oscilloscope U13.54

(c) Oscilloscope U41.54

(d) Oscilloscope U58.54

Figure 49: Comparison of FPGA_CLKIN signal at pin 54 of each FPGA at 90 MHz. In the simulation (top left), the green waveform is U13 pin 54, the pink waveform is U41 pin 54, and the orange waveform is U58 pin 54.

Experimenting with Termination Topologies

Ideally, the FPGA_CLKIN signal path on the CFB would be re-routed, simulated, and the board re-fabricated. Additional time would be required to populate the new board and test for open and/or shorted connections. The material and man-hour costs involved are quite substantial, so various simulations were performed on the FPGA_CLKIN path to establish a possible termination scheme that would reduce signal reflections and increase reliability at higher frequencies. Throughout this pro-

cess, it should be noted that the FPGAs are using the LVCMOS33 logic standard, which indicates that the input logic low threshold voltage is $V_{IL} = 800\,mV$ and the input logic high threshold voltage is $V_{IH} = 2.0\,V$.

The first topology explored was series source termination, which places a resistor in series with the output of the LVDS receiver. In a source termination scheme, the sum of the output impedance of the driver and the terminator should equal Z_0 of the transmission line [12, 16]. The benefit of using source terminators is that it is easier to eliminate reflections because the source typically only has a resistive component in its output impedance, whereas the far end usually has an additional capacitive element [12]. The drawbacks of source termination are slower edge times, and the peak drive current is increased when operating at higher frequencies [12].

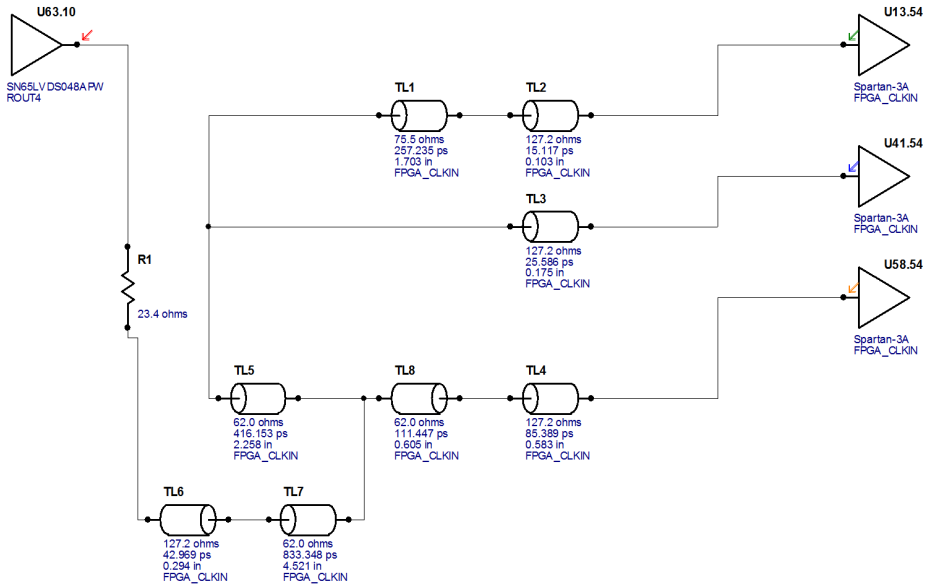
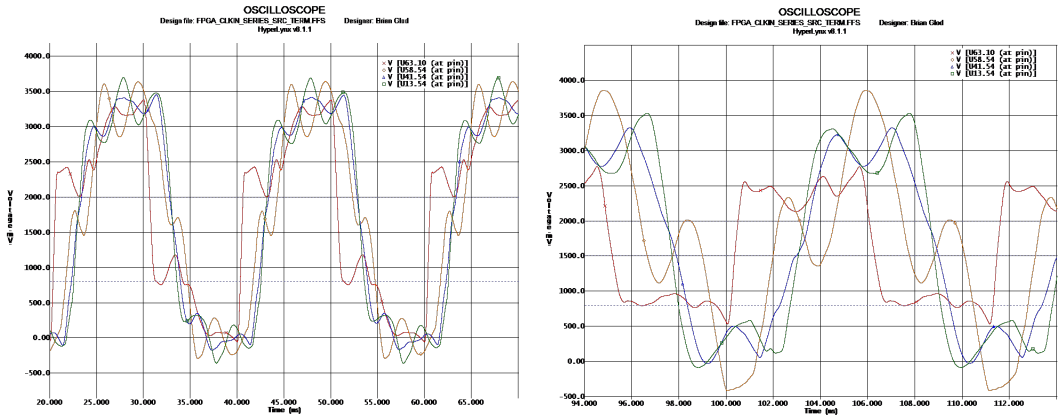


Figure 50: HyperLynx LineSim free-form schematic of FPGA_CLKIN with series source termination.

The HyperLynx termination wizard noted that series termination was optimal and determined that the termination resistance should be $23.4\,\Omega$ as shown in Figure 50. The simulated waveforms using 50 MHz and 90 MHz stimuli are shown in Figure 51.

Comparing the red trace (the output of LVDS receiver U63) in Figure 51b to the same trace in Figure 48b shows that the series source termination significantly increases the signal quality. There is significantly less ringback and the trace more closely resembles a square wave. However, the output of the LVDS receiver is not a critical location. The critical locations are at the input pins of FPGAs U13, U41, and U58. Referring to the 90 MHz orange trace representing U58, the series source termination actually increased the magnitude of the ringback on the rising edge.



(a) 50 MHz (b) 90 MHz

Figure 51: LineSim simulation of the FPGA_CLKIN net at 50 MHz and 90 MHz using series source termination. The red trace is at the output of the LVDS reciever (U63, pin 10). The orange trace is at FPGA U58 pin 54, blue is at FPGA U41 pin 54, and green is at FPGA U13 pin 54.

Another common topology is split termination, or the use of pull-up and pull-down resistors at the receiving end of the transmission line, as shown in Figure 52. The values of the pull-up and pull-down resistors must be such that their parallel combination is equal to Z_0 of the transmission line. This topology is compatible with faster edge times, and due to the split biasing between V_{DD} and ground, logic high and logic low signals have the same power consumption when $R_{pu} = R_{pd}$ [12].

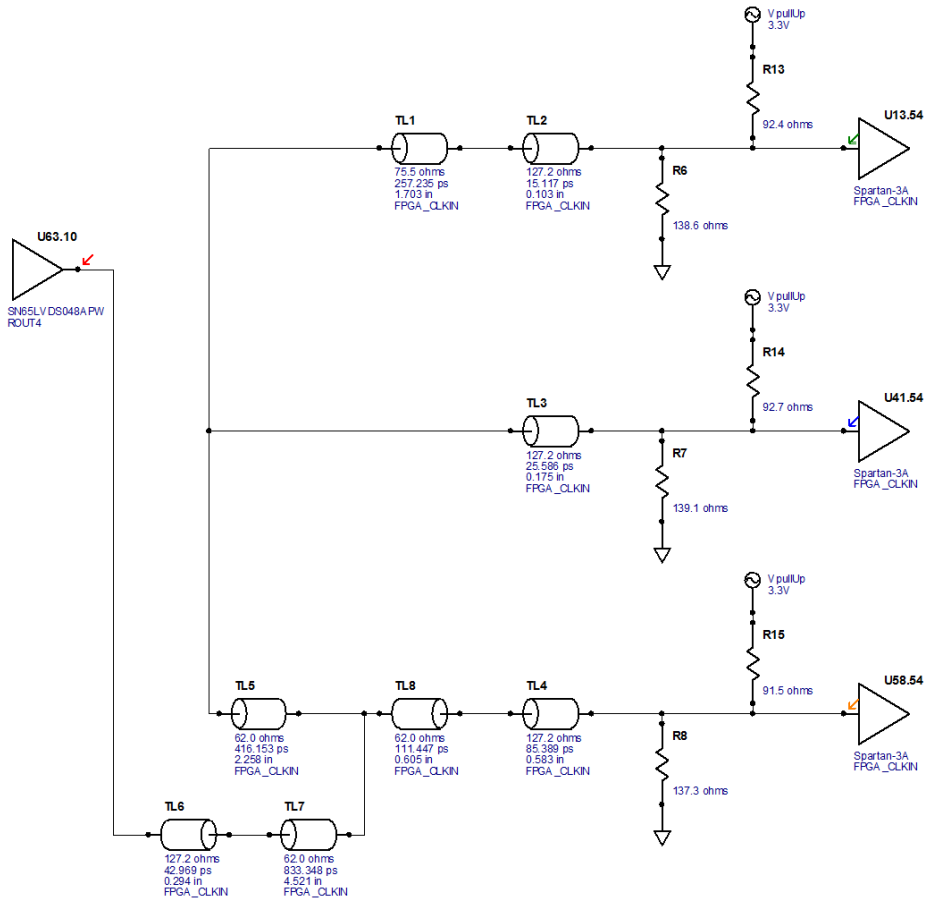
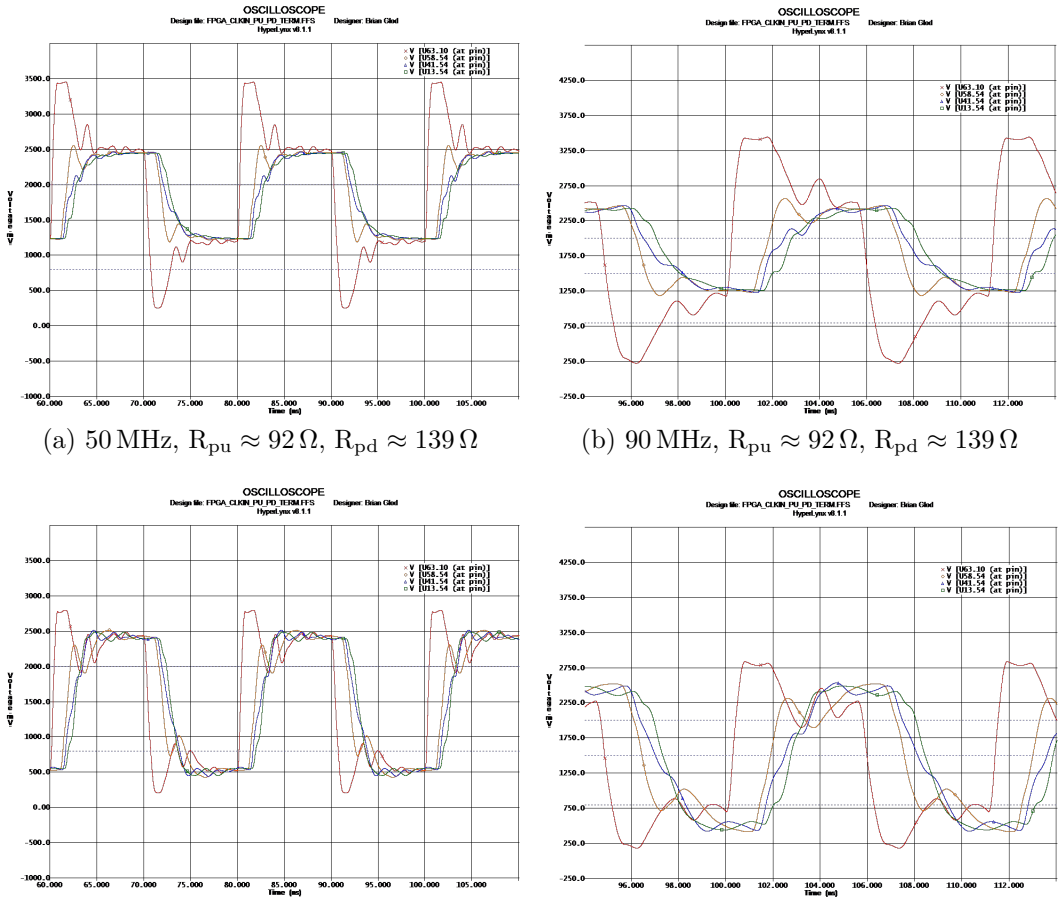


Figure 52: HyperLynx LineSim free-form schematic of FPGA_CLKIN with split end termination. The termination values shown were calculated with the HyperLynx termination wizard.

The HyperLynx termination wizard advised against this topology, but nevertheless provided values that it determined were optimal. In Figures 53a and 53b, the ringback issue was resolved, but came at the expense of not being able to cross the V_{IL} threshold of the FPGAs. Manually adjusting the resistances through a trial-and-error process to $R_{pu} = 300\,\Omega$ and $R_{pd} = 200\,\Omega$ yielded slightly better results, as shown in Figures 53c and 53d. However, these termination values re-introduced the ringback problem, albeit not as severely as before. This topology, combined with the manually

determined termination resistances, could be promising and may be worth further investigation.



(a) 50 MHz, $R_{pu} \approx 92\,\Omega$, $R_{pd} \approx 139\,\Omega$

(b) 90 MHz, $R_{pu} \approx 92\,\Omega$, $R_{pd} \approx 139\,\Omega$

(c) 50 MHz, $R_{pu} = 300\,\Omega$, $R_{pd} = 200\,\Omega$

(d) 90 MHz, $R_{pu} = 300\,\Omega$, $R_{pd} = 200\,\Omega$

Figure 53: LineSim simulation of the FPGA_CLKIN net at 50 MHz and 90 MHz using split end termination. The red trace is at the output of the LVDS reciever (U63, pin 10). The orange trace is at FPGA U58 pin 54, blue is at FPGA U41 pin 54, and green is at FPGA U13 pin 54.

Series end termination as in Figure 54 was also explored even though it is a very non-standard topology. Nevertheless, it appeared to have good results at the inputs to the FPGAs as shown in Figure 55. The ringback completely disappeared and the signal edges transitioned smoothly between V_{IL} and V_{IH}. The primary concern with this configuration is that the logic low state gets close to the absolute minimum input

voltage rating of the FPGAs ($V_{IN,min} = -0.5\,V$). The peak-to-peak input voltage impressed upon the FPGAs can be reduced by increasing the series resistance, but the drawbacks with this approach are similar to the series source termination. Nevertheless, this topology is worth further investigation in terms of hardware implementation and testing.

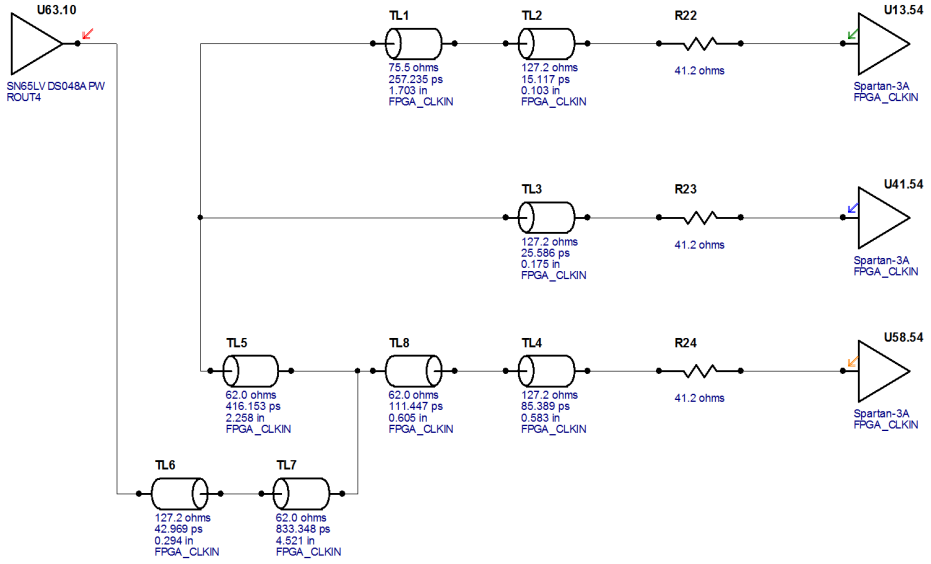
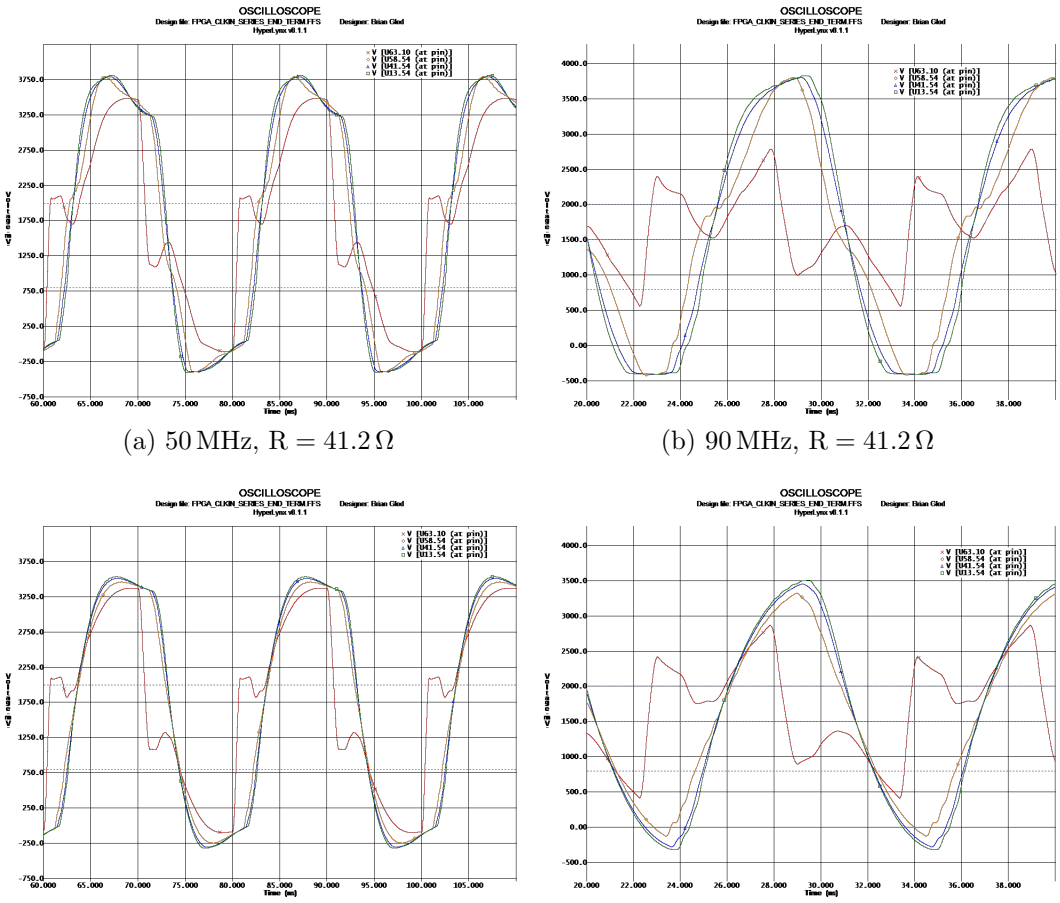


Figure 54: HyperLynx LineSim free-form schematic of FPGA_CLKIN with series end termination. The termination values shown were calculated with the HyperLynx termination wizard.

Additional topologies such as parallel AC end termination, and a combination of series source termination with split end termination were tested, but the results were unremarkable. The parallel AC end termination places a pull-down resistor in series with a capacitor to ground at the far end of the transmission line. The idea behind the use of the capacitor is that, assuming the clock signal has a 50% duty cycle, the capacitor will reach a steady-state charge half-way between V_{DD} and ground [12]. In split termination, one resistor will always have the full V_{DD} across it, but these resistors are twice as big as the single resistor used in the parallel AC termination [12]. The average power dissipation for both topologies are the same,



(a) 50 MHz, R = 41.2 Ω (b) 90 MHz, R = 41.2 Ω

(c) 50 MHz, R = 150 Ω (d) 90 MHz, R = 150 Ω

Figure 55: LineSim simulation of the FPGA_CLKIN net at 50 MHz and 90 MHz using series end termination. The red trace is at the output of the LVDS receiver (U63, pin 10). The orange trace is at FPGA U58 pin 54, blue is at FPGA U41 pin 54, and green is at FPGA U13 pin 54.

and from the perspective of the driver, the two are indistinguishable [12]. However, if the duty cycle does not remain at 50%, the voltage on the capacitor will creep toward one of the extremes. The worst-case drive current would be doubled when switching between logic states and the designer may as well eliminate the capacitor altogether [12]. However, this topology can be useful when configured with a short RC time constant because it helps to guarantee monotonic switching between logic

states [12, 16]. It was in the latter case that this topology was explored, but the ringback/non-monotonicity issue persisted.

While applying termination at one end of the transmission line is sufficient for most applications, the combination of series source termination with the pull-up/pull-down network at the far end can have tremendous benefits, particularly in very high frequency designs. Termination at both ends is extremely tolerant of imperfections within the transmission system and even within the terminators themselves [17]. With higher frequency signals, even small imperfections such as connectors and vias can have a large negative impact in the signal integrity of the system. In this situation, applying termination at both ends will attenuate all secondary reflections caused by the imperfection(s) within the transmission path; this is not possible with any single termination setup [17].

The drawback to using both-end termination is the driver sources a half-amplitude waveform due to the source termination being equal to Z_0, and because of the end termination, this signal remains half-sized, thus a sensitive receiver is required [17]. Note that a driver with only a source terminator sends a half-amplitude signal down the transmission line, but because the other end is effectively an open circuit, the reflected signal is added to the original signal, producing a full-amplitude signal at the receiver [12, 16]. The half-amplitude reflection continues back toward the driver, where it is damped by the series terminator [12, 16]. A driver with split termination at the far end will propagate a full-amplitude signal down the transmission line where it is received full-strength; reflections are attenuated with the pull-up and pull-down network.

5 Conclusion

The initial CFB component population and bench testing was successful. The board appeared to operate properly, but upon deeper analysis with bit error rate testing, eye diagrams, and PCB trace simulation, it became apparent that at least one signal path on the CFB had a major design flaw. The FPGA_CLKIN net on the CFB was not routed with proper attention to high-frequency design strategies. As a result, the clock net exhibited significant signal reflection from impedance discontinuities and excessive trace lengths. Additional testing showed that other nets had signal integrity problems as well, but not nearly as severe as the FPGA_CLKIN net.

With the CFB in its current state, the FPGAs are limited to operating at a maximum frequency of 88 MHz, which corresponds to a detector master clock frequency of 22 MHz—only 2 MHz faster than the minimum required for the Moore and TDEM projects. The BER results with the fast FPGA slew rate showed a small range of frequencies above 88 MHz with zero bit errors, but the stability of these frequencies should be investigated further before using them during detector testing.

Ideally, all problematic traces on the CFB should be re-routed and simulated with HyperLynx prior to future manufacturing. The process would take several weeks or months depending on the number of affected traces. If the CFB were to be re-fabricated, the new board must again pass through the initial inspection, component population, and functionality testing phases. The new PCB would cost nearly $1800 including the various components and military connectors; and the required man-hours would likely bring the total to double that. In an effort to avoid these expenses, this project investigated possible termination schemes that could be implemented on the existing board to rectify the signal integrity problems. Two plausible solutions were proposed.

The first potential termination solution is the use of pull-up/pull-down resistor networks at the far end of the FPGA_CLKIN net near each FPGA input. According to HyperLynx simulations, this solution reduced the ringback and signal reflections, but did not completely eliminate them. The other potential solution would apply series terminators at the far end near the input to each FPGA. This is non-standard and may have implications that were not observed during simulation. Using the series end termination topology, HyperLynx simulations suggested that all reflections and ringback could be eliminated from the input of each FPGA.

In either case, thorough hardware testing should be performed to verify that it is at least possible to correct the problem with a properly routed clock net on the CFB PCB. Unfortunately, because most of the FPGA_CLKIN net is routed on an internal layer, it is simply not feasible to test. Any hardware tests that are performed, however, should use surface mount parts to avoid making the signal integrity problem worse due to the added electrical characteristics of leaded components.

During the course of this study, much was learned in the area of system testing and signal integrity analysis. Signal integrity and high-speed design is not commonly offered in the form of a class. In this case, even though several incorrect hypotheses were made along the way, the process exposed the author to industry-standard circuit board simulation tools, and to ultimately determine a root cause for the signal integrity issues experienced in this design.

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Appendix A

Xilinx Spartan-3 JTAG Configuration Pin Descriptions

The following is adapted from Table 2-15 (pages 66–67) of [4]:

Table A.1: Spartan-3 Generation Configuration Pins

Pin Name	FPGA Direction	Description	During Config.	After Config.
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low.	Drives Low after power-on reset or when PROG_B is pulsed Low while the FPGA is clearing its configuration memory. If a CRC error is detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High or Low to avoid a floating value.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Powered by V_{CCAUX} supply. 0: FPGA not configured, 1: FPGA configured.	Actively drives Low during configuration.	When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins. If driving externally with a 3.3 V output and V_{CCAUX} = 2.5 V, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High during configuration to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA.

Appendix B

Measured System Cable Parameters

Table B.1: System Cabling Measurements: FPGA_DIN

HDL Signal Name	LVDS Drv Signal	100-pin micro-D	Flex Pkg		
Warm Elec Bd	Warm Daughter Bd	Cold Fanout Bd Warm Elec. Bd M83513	Flex Pkg QSH-060	DC Loop Resistance (Ω) Fluke 187 DMM	Capacitance (pF) Agilent U1701A
(meas. offset)	-	-	-	**0.12**	**10.8**
CKDTA_PHASE	CKDTA_PHASE_N	1	77	0.66	92.9
	CKDTA_PHASE_P	27			
GCT	GCT_P	2	84	0.65	91.7
	GCT_N	28			
RR	RR_N	3	81	0.64	91.6
	RR_P	29			
REC	REC_P	4	85	0.65	79.2
	REC_N	30			
PDCKM_1	PDCKM_P_1	5	87-1	0.65	83.4
	PDCKM_N_1	31	88-1		
CDCKM_1	CDCKM_P_1	6	89-1	0.65	80.7
	CDCKM_N_1	32	90-1		
CDMSK_D_3	CDMSK_D_3_N	7	21	0.64	83.0
	CDMSK_D_3_P	33			
CDMSK_D_2	CDMSK_D_2_N	8	22	0.63	82.5
	CDMSK_D_2_P	34			
CDMSK_D_1	CDMSK_D_1_P	9	19	0.63	82.8
	CDMSK_D_1_N	35			
CDMSK_D_0	CDMSK_D_0_P	10	20	0.64	83.6
	CDMSK_D_0_N	36			
CDMSK_DIR	CDMSK_DIR_P	11	26	0.64	86.1
	CDMSK_DIR_N	37			
CDMSK_CKS	CDMSK_CKS_N	12	23	0.65	84.2
	CDMSK_CKS_P	38			
CDMSK_CKL	CDMSK_CKL_P	13	24	0.62	85.1
	CDMSK_CKL_N	39			
CDADDR_CKL	CDADDR_CKL_N	14	45	0.62	82.5
	CDADDR_CKL_P	40			
CDADDR_D	CDADDR_D_P	15	47	0.64	82.6
	CDADDR_D_N	41			
CDADDR_CKS	CDADDR_CKS_N	16	48	0.64	82.2
	CDADDR_CKS_P	42			
CKGEN_ADDR1	CKGEN_ADDR1_P	17	94	0.63	85.4
	CKGEN_ADDR1_N	43			
CKGEN_ADDR0	CKGEN_ADDR0_N	18	96	0.64	82.0
	CKGEN_ADDR0_P	44			
CKGEN_EBL	CKGEN_EBL_P	19	97	0.64	85.0
	CKGEN_EBL_N	45			
CKGEN_GBL	CKGEN_GBL_N	20	98	0.64	82.3
	CKGEN_GBL_P	46			
CKGEN_LOAD	CKGEN_LOAD_P	21	95	0.66	83.1
	CKGEN_LOAD_N	47			
CKGEN_DFLT	CKGEN_DFLT_N	22	93	0.67	84.3
	CKGEN_DFLT_P	48			
CKGEN_CKL	CKGEN_CKL_P	23	91	0.64	86.7
	CKGEN_CKL_N	49			
CKGEN_CKS	CKGEN_CKS_N	24	92	0.67	83.7
	CKGEN_CKS_P	50			
CKGEN_DS	CKGEN_DS_P	25	100	0.68	81.6
	CKGEN_DS_N	51			
PDRST_GBL	PDRST_GBL_N	26	78	0.68	78.2
	PDRST_GBL_P	100			
GCT_GBL	GCT_GBL_P	52	86	0.66	83.2
	GCT_GBL_N	76			
PDCKM_4	PDCKM_N_4	53	87-4	0.65	82.3
	PDCKM_P_4	77	88-4		
CDCKM_4	CDCKM_N_4	54	89-4	0.66	81.2
	CDCKM_P_4	78	90-4		
PDCKM_3	PDCKM_N_3	55	87-3	0.63	82.2
	PDCKM_P_3	79	88-3		
CDCKM_3	CDCKM_P_3	56	89-3	0.63	80.4
	CDCKM_N_3	80	90-3		
PDCKM_2	PDCKM_P_2	57	87-2	0.65	81.3
	PDCKM_N_2	81	88-2		
CDCKM_2	CDCKM_P_2	58	89-2	0.63	83.4
	CDCKM_N_2	82	90-2		
PDPCHG_S_OVR	PDPCHG_S_OVR_P	59	41	0.62	80.3
	PDPCHG_S_OVR_N	83			
PDPCHG_S_IN	PDPCHG_S_IN_P	60	42	0.63	81.5
	PDPCHG_S_IN_N	84			
PDPCHG_N_OVR	PDPCHG_N_OVR_P	61	73	0.62	80.6
	PDPCHG_N_OVR_N	85			
PDPCHG_N_IN	PDPCHG_N_IN_N	62	71	0.63	82.0
	PDPCHG_N_IN_P	86			
CDPCHG_OVR	CDPCHG_OVR_P	63	17	0.63	82.6
	CDPCHG_OVR_N	87			
CDPCHG_IN	CDPCHG_IN_P	64	18	0.62	82.3
	CDPCHG_IN_N	88			
PCHG_ACT	PCHG_ACT_P	65	83	0.61	80.5
	PCHG_ACT_N	89			
RST	RST_N	66	76	0.71	82.8
	RST_P	90			
DISARM_S	DISARM_S_P	67	53	0.62	80.5
	DISARM_S_N	91			
DISARM_N	DISARM_N_N	68	49	0.64	81.8
	DISARM_N_P	92			
ARM_S	ARM_S_P	69	54	0.63	80.9
	ARM_S_N	93			
ARM_N	ARM_N_N	70	52	0.62	83.0
	ARM_N_P	94			
PDOEBL_GBL	PDOEBL_GBL_P	71	82	0.65	79.4
	PDOEBL_GBL_N	95			
DCSEL	DCSEL_N	72	37	0.65	84.3
	DCSEL_P	96			
CDOVR_GBL	CDOVR_GBL_P	73	75	0.64	81.8
	CDOVR_GBL_N	97			
PDOSEL	PDOSEL_N	74	79	0.67	82.9
	PDOSEL_P	98			
PDISEL	PDISEL_P	75	80	0.66	78.7
	PDISEL_N	99			
			Avg.	0.6432	82.926
			Std. Dev.	0.019106575	2.930195369
			Min.	0.61	78.2
			Max.	0.71	92.9

Table B.2: System Cabling Measurements: FPGA_DOUT

PCROIC Signal	Flex Pkg	LVDS Drv Signal	100-pin micro-D		
Flex Pkg TQFP-160	Flex Pkg QSH-060	Cold Fanout Bd	Cold Fanout Bd Warm Elec Bd M83513	DC Loop Resistance (Ω) Fluke 187 DMM	Capacitance (pF) Agilent U1701A
(meas. offset)	**-**	**-**	**-**	**0.12**	**10.8**
PDDTA_7	68	PDDTA_7_N	1	0.64	82.4
		PDDTA_7_P	27		
PDDTA_6	63	PDDTA_6_P	2	0.64	79.8
		PDDTA_6_N	28		
PDDTA_5	64	PDDTA_5_P	3	0.62	80.8
		PDDTA_5_N	29		
PDDTA_4	59	PDDTA_4_P	4	0.63	84.5
		PDDTA_4_N	30		
PDDTA_3	60	PDDTA_3_P	5	0.62	80.4
		PDDTA_3_N	31		
PDDTA_2	55	PDDTA_2_N	6	0.62	78.4
		PDDTA_2_P	32		
PDDTA_1	56	PDDTA_1_P	7	0.62	79.3
		PDDTA_1_N	33		
PDDTA_0	51	PDDTA_0_N	8	0.61	79.8
		PDDTA_0_P	34		
CDDTA_CKS_REF	46	CDDTA_CKS_REF_P	9	0.61	80.8
		CDDTA_CKS_REF_N	35		
CDDTA_15	43	CDDTA_15_N	10	0.62	79.6
		CDDTA_15_P	36		
CDDTA_14	44	CDDTA_14_P	11	0.60	80.5
		CDDTA_14_N	37		
CDDTA_13	39	CDDTA_13_N	12	0.60	76.2
		CDDTA_13_P	38		
CDDTA_12	40	CDDTA_12_P	13	0.60	78.1
		CDDTA_12_N	39		
CDDTA_11	38	CDDTA_11_N	14	0.61	81.6
		CDDTA_11_P	40		
CDDTA_10	35	CDDTA_10_P	15	0.60	78.5
		CDDTA_10_N	41		
CDDTA_9	36	CDDTA_9_N	16	0.61	80.0
		CDDTA_9_P	42		
CDDTA_8	33	CDDTA_8_P	17	0.60	81.5
		CDDTA_8_N	43		
CDDTA_7	34	CDDTA_7_N	18	0.62	81.8
		CDDTA_7_P	44		
CDDTA_6	31	CDDTA_6_P	19	0.65	80.8
		CDDTA_6_N	45		
CDDTA_5	32	CDDTA_5_N	20	0.63	82.0
		CDDTA_5_P	46		
CDDTA_4	29	CDDTA_4_P	21	0.63	79.8
		CDDTA_4_N	47		
CDDTA_3	30	CDDTA_3_N	22	0.64	78.7
		CDDTA_3_P	48		
CDDTA_2	27	CDDTA_2_P	23	0.62	80.8
		CDDTA_2_N	49		
CDDTA_1	28	CDDTA_1_N	24	0.66	79.3
		CDDTA_1_P	50		
CDDTA_0	25	CDDTA_0_P	25	0.65	82.5
		CDDTA_0_N	51		
			26	0.66	79.4
			100		
PDDTA_9	57	PDDTA_9_P	52	0.64	83.6
		PDDTA_9_N	76		
FPGA_DIN_7		FPGA_DIN_7_N	53	0.64	82.7
		FPGA_DIN_7_P	77		
FPGA_DIN_6		FPGA_DIN_6_P	54	0.64	85.6
		FPGA_DIN_6_N	78		
FPGA_DIN_4		FPGA_DIN_4_P	55	0.62	82.6
		FPGA_DIN_4_N	79		
FPGA_DIN_5		FPGA_DIN_5_P	56	0.62	82.9
		FPGA_DIN_5_N	80		
FPGA_DIN_3		FPGA_DIN_3_N	57	0.62	82.9
		FPGA_DIN_3_P	81		
FPGA_DIN_2		FPGA_DIN_2_P	58	0.61	83.4
		FPGA_DIN_2_N	82		
FPGA_DIN_1		FPGA_DIN_1_P	59	0.61	84.0
		FPGA_DIN_1_N	83		
FPGA_DIN_0		FPGA_DIN_0_N	60	0.62	81.4
		FPGA_DIN_0_P	84		
FPGA_CLKIN		FPGA_CLKIN_P	61	0.61	83.2
		FPGA_CLKIN_N	85		
PDPCHG_S	42	PDPCHG_S_OUT_P	62	0.61	82.5
		PDPCHG_S_OUT_N	86		
PDPCHG_N	71	PDPCHG_N_OUT_N	63	0.60	84.4
		PDPCHG_N_OUT_P	87		
CDPCHG	18	CDPCHG_OUT_P	64	0.59	81.8
		CDPCHG_OUT_N	88		
PD_SYNC	72	PD_SYNC_N	65	0.60	83.8
		PD_SYNC_P	89		
PDDTA_8	58	PDDTA_8_P	66	0.62	81.1
		PDDTA_8_N	90		
PDDTA_S_CKS_REF	74	PDDTA_S_CKS_REF_N	67	0.60	83.1
		PDDTA_S_CKS_REF_P	91		
PDDTA_N_CKS_REF	50	PDDTA_N_CKS_REF_P	68	0.61	82.9
		PDDTA_N_CKS_REF_N	92		
PDDTA_15	69	PDDTA_15_N	69	0.61	84.1
		PDDTA_15_P	93		
PDDTA_14	70	PDDTA_14_P	70	0.62	82.4
		PDDTA_14_N	94		
PDDTA_13	65	PDDTA_13_N	71	0.62	81.9
		PDDTA_13_P	95		
PDDTA_12	66	PDDTA_12_P	72	0.63	81.2
		PDDTA_12_N	96		
PDDTA_11	61	PDDTA_11_N	73	0.62	82.4
		PDDTA_11_P	97		
PDDTA_10	62	PDDTA_10_P	74	0.64	83.3
		PDDTA_10_N	98		
CD_SYNC	67	CD_SYNC_N	75	0.65	83.2
		CD_SYNC_P	99		
			Avg.	0.6212	81.554
			Std. Dev.	0.016980181	1.941408073
			Min.	0.59	76.2
			Max.	0.66	85.6

Appendix C

HyperLynx TechNote MG243236

The following is quoted from [18]:

> Cable Models in HyperLynx today are lossless just like the Simple Transmission Line Model and is not based on the stackup.
>
> In order to model a lossy cable ask your vendor for a SPICE or S-parameter model for your cable. You can assign these types of models to the package/connector symbol in LineSim to simulate a cable using the ADMS simulator.
>
> Another option is to model a transmission line using the stackup and adjusting it to get your desired impedance, delay and loss that is equivalent to the characteristics of your cable. Follow these steps to get the correct stackup parameters.
>
> 1. Use an internal layer configured as a symmetric stripline in the stackup. Change the dielectric thickness above and below the signal layer so the distance between reference planes is nearly the same as the diameter of the cable you are modeling.

2. Place a transmission line symbol in LineSim and change its parameters to place that trace on the target internal layer. This transmission line symbol will report to you the electrical parameters as you adjust the physical parameters.
3. Change the dielectric constant of the layers above and below the symmetric stripline layer so that the propagation delay of a trace on that internal layer is equal to the propagation delay of your cable.
4. Adjust the trace width to make the trace impedance match that of the cable.
5. Adjust the metal resistivity so that the DC resistance matches the cable specification.
6. Adjust the dielectric loss tangent to make the trace loss match the loss specified for the cable at whatever frequency the specification states.

This method works equally well for twisted pair cables in signal integrity simulations. Since the 2-D model does not include the twisting of the cable, this method does not apply to EMI analysis.

An enhancement request has been entered for the ability to specify lossy cable parameters.

Appendix D

Twisted Pair Transmission Line Equations

The following equations are adapted from [12]:

Table D.1: Variables used

d	diameter of wire (in.)
s	separation between wires (in.)
x	length of wire (in.)
$\epsilon_{r,eff}$	effective relative dielectric constant of medium between wires

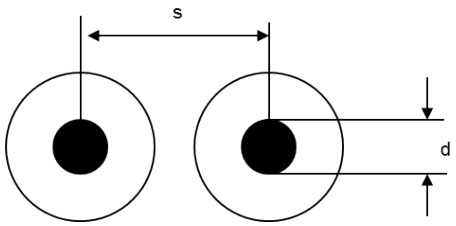


Figure D.1: Depiction of the variables used in the following equations.

Characteristic impedance of twisted pair (Ω):

$$Z_0 = \frac{120}{\sqrt{\epsilon_{r,eff}}} \cdot \ln\left[\frac{2 \cdot s}{d}\right] \tag{D.1}$$

Propagation delay per inch of twisted pair (sec./in.):

$$t_{pd} = (84.72 \times 10^{-12}) \cdot \sqrt{\epsilon_{r,eff}} \tag{D.2}$$

Inductance of twisted pair (H):

$$L = x \cdot 10.16 \cdot 10^{-9} \cdot \ln\left[\frac{2 \cdot s}{d}\right] \tag{D.3}$$

Capacitance of twisted pair (F):

$$C = \left[\frac{x \cdot 0.7065 \cdot 10^{-12}}{\ln\left[\frac{2 \cdot s}{d}\right]}\right] \cdot \epsilon_{r,eff} \tag{D.4}$$

UTP Calculations for the Section of Warm Cable

Twisted by RIT Center for Detectors using cordless drill and hand-soldered.

Manufacturer:	Glenair
Model:	M83513/04-H14N
Wire specifications:	M22759/11-26; Teflon insulated

$d = 26$ AWG, str. $= 0.0185$ in.
$s \approx 0.06$ in.
$x = 72$ in.
$\epsilon_{r,eff} \approx 1.8$
$\varnothing_{\text{outer}} = 40.5$ mil

$Z_0 = 167.23\Omega$
$L = 1.37\,\mu\text{H}$
$C = 48.97\,\text{pF}$
$t_{pd} = 0.113\,66\,\text{ns/in.}$
$t_{pd} = 8.184\,\text{ns (total)}$

UTP Calculations for the Section of Cold Cable

Professionally twisted and soldered by Universal Cryogenics.

Manufacturer:	Glenair
Model:	M83513/04-H03N
Wire specifications:	M22759/11-26; Teflon insulated

$d = 26$ AWG, str. $= 0.0185$ in.
$s \approx 0.0435$ in.
$x = 14$ in.
$\epsilon_{r,eff} \approx 1.9$
$\varnothing_{\text{outer}} = 40.5$ mil

$Z_0 = 134.78\Omega$
$L = 0.220\,\mu\text{H}$
$C = 12.14\,\text{pF}$
$t_{pd} = 0.116\,78\,\text{ns/in.}$
$t_{pd} = 1.635\,\text{ns (total)}$

UTP Calculations Category 5e Cable

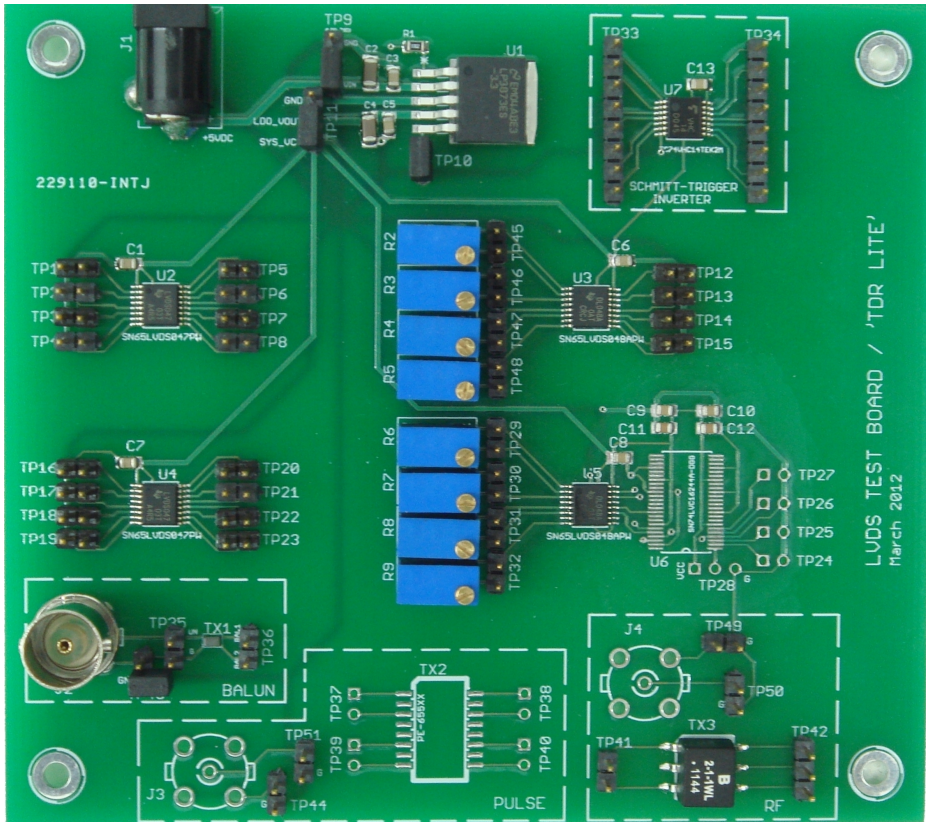
Professionally twisted; sheathing label: "GrandMax UTP Cat.5e/350 MHz Patch ISO/IEC 11801 & EN 50288 & TIA/EIA-568-B.2 ETL/3P Verified For Gigabit Ethernet 24 AWG x 4P Type CM(UL) C(UL) CMH E164469-F3 RoHS"

$d = 24$ AWG, str. $= 0.0232$ in.
$s \approx 0.038$ in.
$x = 313$ in.
$\epsilon_{r,eff} \approx 2.2$
$\varnothing_{\text{outer}} = 38.0$ mil

$Z_0 = 96.0\Omega$
$L = 3.773\,\mu\text{H}$
$C = 409.9\,\text{pF}$
$t_{pd} = 0.125\,66\,\text{ns/in.}$
$t_{pd} = 39.33\,\text{ns}$ (total)

Appendix E

LVDS Test Board Information



For proper operation of the National Semiconductor LP3873 LDO regulator, the ~SD pin must be pulled high (to V_{IN}, not to exceed 7.5 V_{DC}) through a 10 kΩ resistor

(TP9). Additionally, if not used, the ~ERROR pin must be pulled to ground (TP10). A "star ground" topology was used to help reduce potential ground currents that could cause instability in the regulator or noise in the system.

The TP11 jumper optionally connects the regulated 3.3 V_{DC} output of the LDO to the V_{CC} pins of each component on the board by shorting LDO_VOUT to SYS_VCC. Alternatively, it provides convenient connection points (SYS_VCC and GND) for applying power via external voltage sources such as a bench-top supply. The design of this board makes it easy to accidentally short the LDO output to ground through the TP11 jumper. This was known at design time, but deemed an acceptable risk in order to reduce jumper pins while quickly and conveniently providing connection points for alternative voltage sources. Ordinarily this is not the best design practice, but the justification is primarily due to the LDO having short-circuit protection. In the event TP11 shorts LDO_VOUT and GND, the LDO will abruptly turn itself off and prevent damage as long as the short-circuit current remains below 6 A. The intended wall-wart power supply is an Emerson DA12-050US-M, which is rated for 2 A at 5 V. This supply also features overload and short-circuit protection that activates at 2.5 A, well before the LDO can reach its 6 A limit. Additionally, all of the power interconnects and jumpers were selected to have a minimum current rating of 3 A.

The components marked U2 and U3 are the Texas Instruments SN65LVDS047PW and SN65LVDS048APW LVDS driver and receiver chips, respectively. These are the same components used in the imaging system. The supply bypass capacitors are 0.1 µF and are the same as those used in the imaging system. The Vishay M64Y102KB40 potentiometers labeled R2 through R9 are used to tune the optimal termination at the receivers. (Note that the LVDS chips have a fail-safe that prevents damage if the termination is left open, or shorted). In the imaging system, static 100 Ω resistors are used instead.

Below the U2 and U3 group, there is a second pair of LVDS driver and receiver modules at U4 and U5. In this grouping, there is the addition of U6, the 16-bit buffer/driver chip TI SN74LVC16244A. This chip is used in the imaging system to adequately drive four detectors simultaneously without signal degradation; it also provides a means to enable or disable control signals to each detector. The footprint for this chip was left unpopulated because it was unclear whether it was necessary.

At the bottom of the board are three different transformer configurations. These transformers exist for testing various TDR design configurations. The transformer located at TX1 (Murata DXW21BN7511TL) is a standard balun transformer, named as such because it is used specifically for converting signals to and from BALanced (i.e. differential) and UNbalanced (i.e. single-ended). Positions TX2 and TX3 are inexpensive pulse and RF transformers, Pulse PE-65508 and Bourns 2-1-1WL, respectively.

Per the datasheet, the signal generator available at CfD has an approximate edge time of 5 ns. This might be too slow for the (relatively short) cable lengths of interest, so a Toshiba TC74VHC14FTEK2M Schmitt-trigger inverter was added (top right of Figure 30) to help increase the edge time. The output of the Schmitt-trigger can be connected to one of the transformers and assist in obtaining a TDR measurement.

The BNC connectors near the transformers provide convenient hook-ups to external lab equipment. There are also standard 100 mil headers for alternative connection possibilities. In general, each transformer "block" has the same connection configuration. Looking at the PULSE block: TP44 is used to optionally connect the BNC shell/shield to system ground; and TP51 can be used for feeding in signals from other equipment that may not utilize BNC connections. Either TP51 or BNC J3 should be used for providing input signals, not both. However, one can be used as an input, and the other can be used for signal monitoring with an oscilloscope.